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Attorneys for Defendant
UNITED MICROELECTRONICS CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

MICRON TECHNOLOGY, INC.,

Plaintiff,

v.

UNITED MICROELECTRONICS CORPORATION, FUJIAN JINHUA INTEGRATED CIRCUIT CO., LTD., and DOES 1-10,

Defendants.

Case No. 3:17-CV-06932-MMC

DECLARATION OF ROBERT G. LITTS IN SUPPORT OF DEFENDANT UNITED MICROELECTRONICS CORPORATION'S MOTION TO DISMISS PLAINTIFF MICRON TECHNOLOGY, INC.'S SECOND AMENDED COMPLAINT

Judge: Hon. Maxine M. Chesney
Courtroom: 7 – 19th Floor
Hearing Date: July 12, 2019
Hearing Time: 9:00 a.m.

SAC Filed: May 24, 2019

I, Robert G. Litts, declare as follows:

1. I am an attorney licensed to practice law in the State of California, and I am admitted to practice before this Court. I am a partner at Dan Johnson Law Group, LLP, and I am one of the attorneys representing United Microelectronics Corporation in the above-captioned matter. I make this declaration on personal knowledge, and if called as a witness, I could and would competently testify with respect to the matters stated herein.

2. Attached hereto as Exhibit **1** is a true and correct copy of U.S. Patent No. 3,387,286.

3. Attached hereto as Exhibit **2** is a true and correct copy of U.S. Patent No. 5,398,205.

4. Attached hereto as Exhibit **3** is a true and correct copy of U.S. Patent No. 8,048,737.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct to the best of my knowledge and belief.

Executed this 7th day of June 2019, in South San Francisco, California.

DAN JOHNSON LAW GROUP

/s/ *Robert G. Litts*
Robert G. Litts (Bar No. 205984)

Exhibit 1

June 4, 1968 R. H. DENNARD 3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Filed July 14, 1967 3 Sheets-Sheet 1

FIG. 1

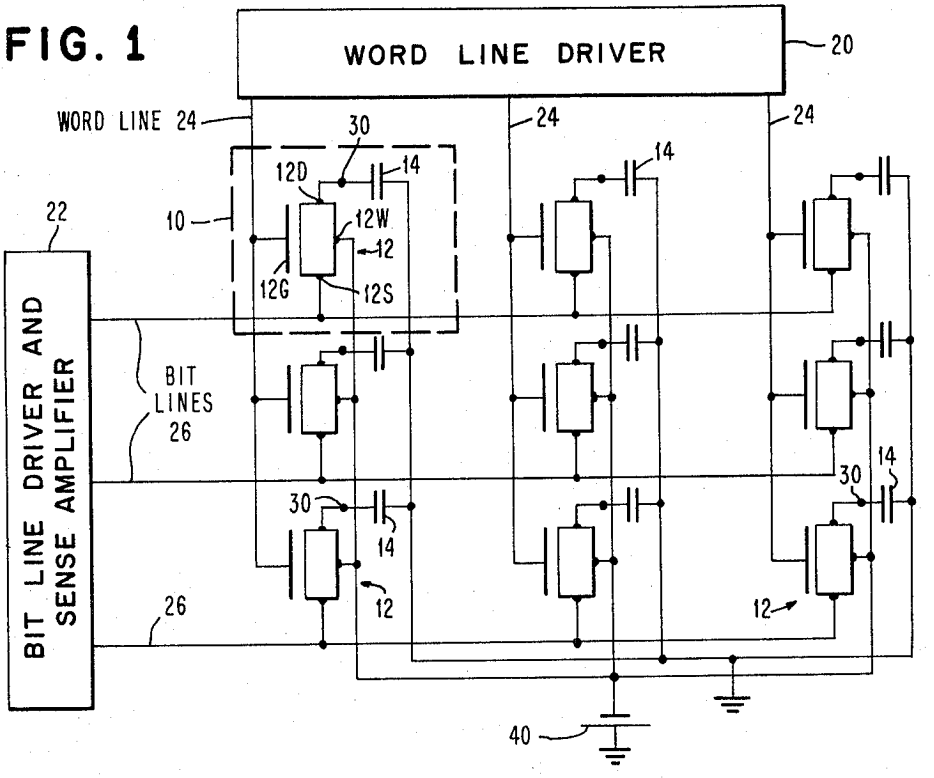
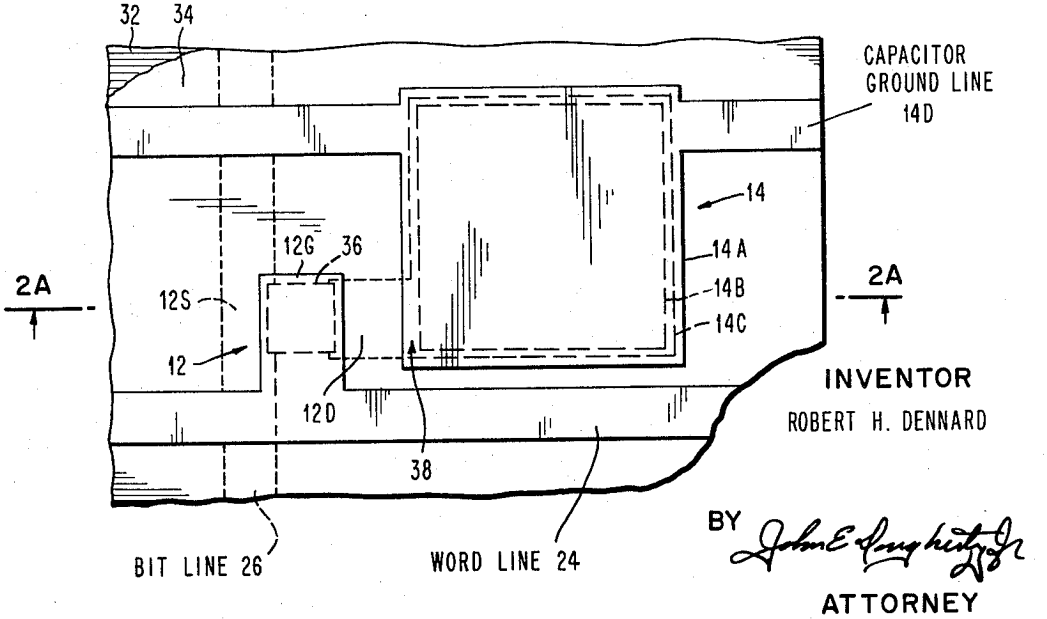


FIG. 2



INVENTOR
ROBERT H. DENNARD

BY John E. Laughlin Jr.
ATTORNEY

June 4, 1968 R. H. DENNARD 3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Filed July 14, 1967 3 Sheets-Sheet 2

FIG. 2A

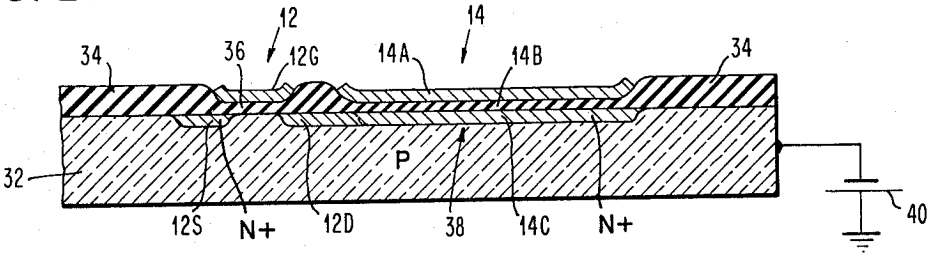
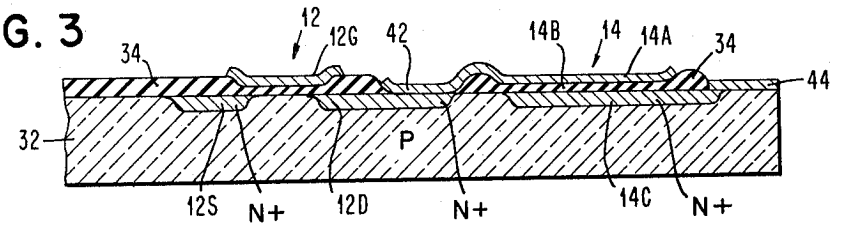


FIG. 3



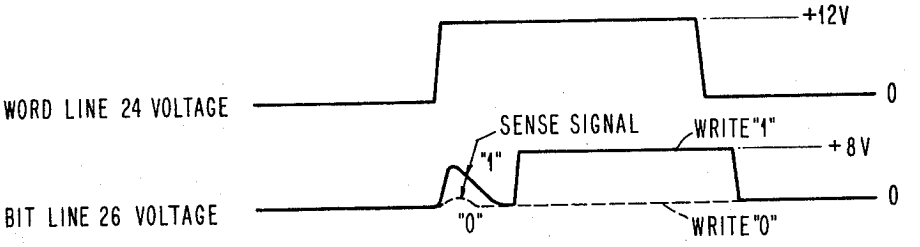


FIG. 4A

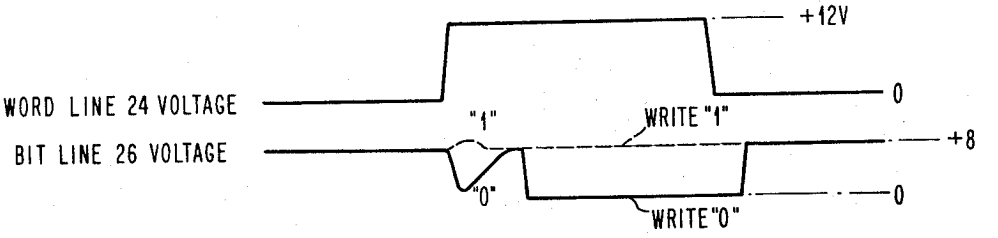


FIG. 4B

June 4, 1968 R. H. DENNARD 3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Filed July 14, 1967 3 Sheets-Sheet 3

FIG. 5

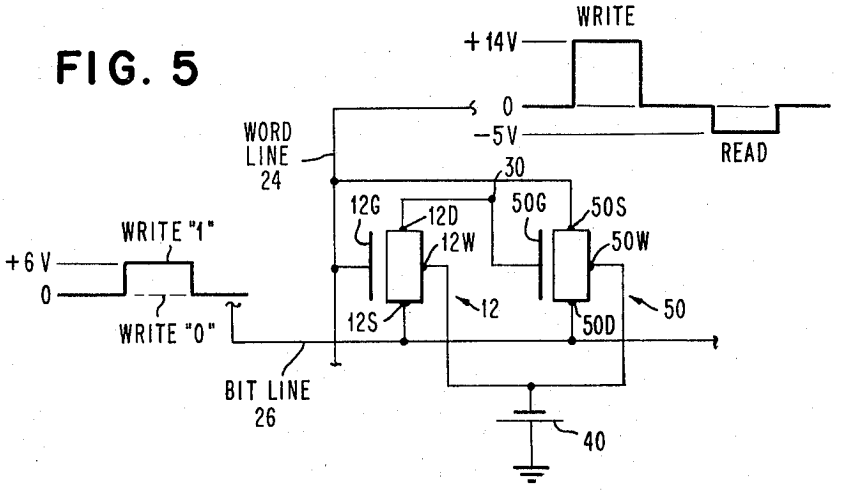


FIG. 7

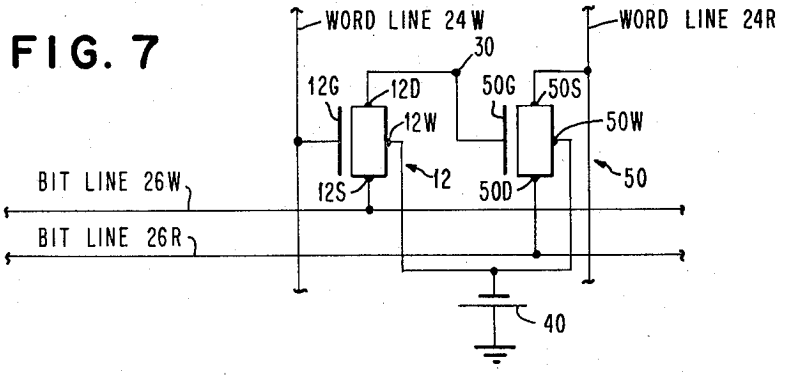
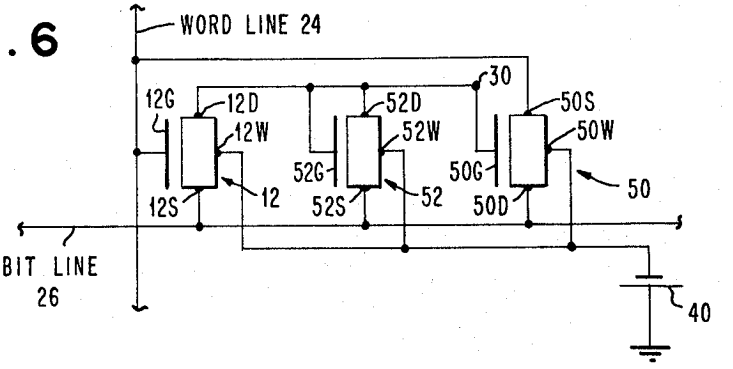


FIG. 6



United States Patent Office 3,387,286 Patented June 4, 1968

3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Robert H. Dennard, Croton-on-Hudson, N.Y., assignor to International Business Machines Corporation, Armonk, N.Y., a corporation of New York

Filed July 14, 1967, Ser. No. 653,415
21 Claims. (Cl. 340—173)

ABSTRACT OF THE DISCLOSURE

The memory is formed of an array of memory cells controlled for reading and writing by word and bit lines which are connected to the cells. Each cell is formed, in one embodiment, using a single field-effect transistor and a single capacitor. The gate electrode of the transistor is connected to the word line, the source terminal to the bit line, and the drain terminal directly to one of the electrodes of the capacitor. The other electrode of the capacitor is connected to a reference potential. Information is stored by charging the capacitor through the transistor and information is read out by discharging the capacitor through the transistor. During a write operation the word line, which is connected to the gate of the transistor, is energized to render the transistor conductive between source and drain. If a zero is to be stored, the bit line is not energized and the capacitor is not charged. If a one is to be stored, the bit line is energized and the capacitor is charged to essentially the potential of the bit line signal. During read operations only the word line is energized and a signal is transmitted to the bit line if a one has been stored previously and the capacitor is charged. Since the charge on the capacitor does leak off, it is necessary to periodically regenerate the information stored in the memory.

In another disclosed embodiment rather than storing a charge in a conventional capacitor, a second field-effect transistor is used and the charge is stored in the capacitance between the gate and substrate of this transistor. In this memory the readout is nondestructive with the charge stored at the gate of the second transistor being used to render that transistor conductive when a binary one is stored, so that the word line signal is transmitted through this second transistor to the bit sense line. The entire memory in these and other embodiments disclosed is preferably fabricated in integrated circuit form using a single substrate of semiconductor material.

Prior art

Pertinent prior art is as follows:

(a) "Integrated High-Speed, Read-Only Memory with Slow Electronic Write" by A. S. Farber, IBM Technical Disclosure Bulletin, vol. 8, No. 3, August 1965.

(b) "Nondestructive Readout Memory Cell Using MOS Transistor" by P. Pleshko, IBM Technical Disclosure Bulletin, vol. 9, No. 8, January 1966.

(c) "Integrated MOS Transistor Random Access Memory" by J. D. Schmidt, Solid State Design, January 1965.

(d) Application Ser. No. 403,482, filed Oct. 13, 1964, on behalf of Arnold Farber et al. and commonly assigned.

As is shown in the above art, memories have been built using field effect transistors. Further, as is disclosed in the co-pending application of Farber et al., the capacitance of a field-effect transistor has been employed to store information in a shift register.

A further publication indicating current work in the use of field-effect transistors operated in a storage mode in a photodetector is found in an article by G. P. Weckler, which appeared on page 75 of Electronics, May 1, 1967.

Though the above art and current publications are pertinent in disclosing various concepts and structures which have been developed in the application of field-effect transistors to different types of memory applications, the primary thrust up to this time in conventional read-write random access memories has been to connect a plurality of field-effect transistors in each cell in a latch configuration. Memories of this type require a large number of active devices in each cell and therefore each cell requires a relatively large area on the integrated circuit substrate. This type of design limits the number of memory cells which can be built on a single substrate and further necessitates the use of longer drive and sense lines at the expense of speed of operation of the memory.

Summary of the invention

In the present invention a random access memory is provided in an integrated circuit structure in which each cell requires a minimum of two components. Since only two components are required, the area per cell on the substrate is extremely small and a very large memory including many cells can be built on a single substrate and operated at very high speeds. In the memory of the present invention the binary information is stored by storing a charge on a capacitor which is either an integrated circuit capacitor or the gate to substrate capacitance of a field-effect transistor. Though this type of storage is not remanent in the same sense as storage in a latch type circuit or a magnetic core, since the charge tends to leak off with time, the time during which the stored charge remains at a satisfactory value has been found to be very long compared with the read-write cycle time for the memory. Thus even though in the inventive memory it is necessary to periodically regenerate the stored information, the regeneration need occupy only 10 to 20% of the time and the memory is used for conventional operations during the remaining 80% of the time. Read-write cycles of 100 nanoseconds are achievable and, even though regeneration is necessary, the total effect is to provide a memory which has a read-write cycle time, in terms of actual use, in the vicinity of 120 nanoseconds.

The minimum number of components, either two field-effect transistors or one field effect transistor and a capacitor for each memory cell, is achieved by designing the circuit so that one transistor which serves as an input transistor controls both the charging of the capacitor during writing and the interrogation of the capacitor during reading. Where the second element in the cell is a conventional capacitor, the read out is destructive, but where the second element is another field-effect transistor, nondestructive read out can be achieved.

Therefore it is an object of the present invention to provide an improved memory which can be mass fabricated in integrated circuit form.

It is a further object of the present invention to provide a memory of the above described type which requires a minimum of components in each memory cell in the memory.

Another object is to provide an integrated circuit memory which dissipates very little power.

A more specific object is to provide an integrated circuit memory which does not require the application of power to the storage cells to retain information in the memory.

It is a further object of the present invention to provide an integrated circuit memory in which each cell of the memory requires a very small area of the integrated circuit wafer, thereby allowing the memory cells to be placed on the wafer with an extremely high density.

It is still a further object of the present invention to provide a random access memory using integrated circuit techniques in which the total effective speed for read and write operations in the memory is extremely fast even

though periodic regeneration of the stored information in the memory is necessary.

It is still a further object of the present invention to provide an improved integrated circuit memory in which information is stored in a capacitor formed on one surface of the memory chip, and wherein the structure is so designed so as to take full advantage of the relatively large capacitance of this capacitor and avoid limiting the capacitive action by the stray capacitances inherent in the integrated structure.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

Brief description of the drawings

FIG. 1 is a partly schematic diagram illustrating the electrical connections of a memory built in accordance with the principles of the present invention.

FIGS. 2 and 2A are respectively top and sectional views of one embodiment of a memory cell for the circuit of FIG. 1 where the cell formed in an integrated circuit on a single substrate.

FIG. 3 is a sectional view illustrating another embodiment in integrated circuit form of a memory cell for the memory of FIG. 1.

FIGS. 4A and 4B illustrate two different modes of applying signals to the word and bit lines of the memory of FIG. 1 to carry out read and write operations in that memory.

FIGS. 5, 6 and 7 are electric circuit diagrams showing three other embodiments of memory cells constructed in accordance with the principles of the present invention.

Description of the preferred embodiments

The memory shown in FIG. 1 is a three by three array of nine memory cells **10**, each of which is formed of a field-effect transistor **12** and a capacitor **14**. Only nine cells are shown in this embodiment, since this is all that is required to illustrate the principles of the invention. In actual practice, of course, much larger memories including many more memory cells are employed, but the showing of such a large embodiment, though more realistic in terms of actual use, would only serve to complicate the disclosure without adding to the teaching. Each transistor **12** in each memory cell **10** includes a gate electrode **12G** to which signals are applied to control current flow between a source terminal **12S** and a drain terminal **12D**. A further connection is made to the substrate or wafer on which the field effect devices are formed and this connection is shown at **12W**. Each of these transistors is an insulated-gate field-effect transistor. Transistors of this type are also known as MOS or metal-oxide-semiconductor transistors. All the transistors are formed on a wafer or substrate of silicon which is P type. The source and drain regions are doped to be N type, and are at the surface to provide planar construction. These two regions are connected by a channel at the surface of the substrate wafer which is located immediately beneath the gate electrode **12G**. The transistors are enhancement type, by which it is meant that the channel between the source and drain regions is normally nonconducting and is rendered conductive by the application of a positive signal to the gate electrode **12B**. For conduction to occur there must be a voltage difference between the source and drain terminals, and the gate voltage must exceed the voltage at the more negative of these terminals, the source terminal, by the threshold voltage for the transistor. The practice of the invention is not limited to enhancement mode NPN structures, since PNP field-effect devices can also be used. Depletion mode devices, in which the channel between source and drain is normally conducting and is rendered nonconductive by gate signals, can also be employed with appropriate changes in the voltages applied to the circuitry for controlling the memory array.

The operation of the memory of FIG. 1 to read and write information in the memory cells **10** is controlled by word line drivers, represented by block **20**, and bit line drivers and sense amplifiers, represented by block **22**. There are three word lines **24**, one for each vertical column or word position in the array and three bit lines **26**, one for each horizontal row or bit position in the array. The memory is word organized and is operated on a read-write cycle basis. Specifically, during the first or read portion of the cycle, the information bits stored in the three cells of one of the three vertically extending words are read out by the application of a signal to the appropriate word line **24**. Signals representative of stored information are transmitted via bit lines **26** to the sense amplifiers. During the latter portion of each read-write cycle, the same or new information is written into the same word position by the application through the bit lines drivers of appropriate signals to bit line **26**. Two different pulse patterns which may be employed are illustrated in FIGS. 4A and 4B. The sense signals are shown in these figures to be much larger in amplitude relative to the drive signals than is the actual case. The operation of the individual cells in the memory may be understood from the following description of the operation of the cell **10** shown at the upper left hand portion of the array of FIG. 1.

Referring specifically to the memory cell in the upper left hand corner of FIG. 1, the information, binary one or binary zero, stored in this cell is determined by the voltage at a storage node **30**. When storing a binary zero, the voltage at node **30** is low and there is essentially no charge on capacitor **14**. When storing a binary one, the voltage at storage node **30** is at a higher positive value and capacitor **14** is charged. Thus the storage element in the memory cell is the capacitor **14** and a binary one or a binary zero is stored in the cell according to whether or not this capacitor is charged. In the normal state of the cell, between read and write operations on the cell, a charge stored on capacitor **14** is maintained due to the fact that the circuit in which the capacitor is connected extends through the transistor **12**. This transistor is normally in its off condition and presents an extremely high impedance in the circuit. Thus though there is some leakage across the drain junction in the transistor and through the body of the substrate to the substrate terminal **12W**, a charge on capacitor **14** can be stored for a relatively long time compared to the time required for a read-write operation.

During a read-write operation carried on in the first word position in the memory, the appropriate word line **24** is energized with a positive pulse as is indicated in FIG. 4A. This voltage is applied to the gates **12G** for each of the transistors in the first column of the array. The voltage applied to each gate causes the channel connecting the source and drain regions in the transistor to be conductive. Assume that a binary one is stored in the cell under consideration. Capacitor **14** is then charged and when transistor **12** is rendered conductive, capacitor **14** discharges through the conductive transistor and delivers a signal to the bit line **26**, which is connected to the source terminal **12S** for the transistor. This signal is transmitted via line **26** to the sense amplifier for the first bit position in the array and from this amplifier can be detected and transmitted to other portions of data processing equipment in which the memory is used. If the word line signal is applied to line **24** and a binary zero is stored in the cell, capacitor **14** has little or no charge and the storage node **30** is at a low voltage. No signal is then delivered through the conductive transistor **12** to the bit line indicating the presence of a binary zero in the cell. It should be noted that only cells of the selected word are connected to the bit line during reading, and other cells having their word lines de-energized cannot either deliver or absorb current into or from the bit line.

Upon completion of the initial portion of the read-write cycle, new information is written into the cells in the

first column of the array by the application of appropriate signals to the bit lines **26** under the control of the bit drivers represented in block **22**. The signals applied to bit lines **26** may represent the same informaton which was originally stored in the first column of the array or new information may be written. The operation here of the sense amplifiers and the bit line drivers in applying information signals to line **26** is the same as is used in cenventional memories and is therefore not shown in detail. When a binary one is to be written during the latter portion of the read-write cycle, a positive signal is applied to the appropriate bit line **26**. When a binary zero is to be written, the line **26** is maintained at essentially zero potential. During the latter portion of the read-write operation, as is indicated in FIG. 4A, the write line voltage is maintained, and the transistor **12** remains conductive between source and drain. Thus the signal applied to the bit line **26** charges the capacitor **14** to either the zero voltage level of the higher positive voltage level representative of a binary one according to the voltage applied to the bit line **26**. The write signal on line **24** is maintained for a time sufficient to fully charge capacitor **14**, at which time the word line voltage is terminated thereby removing the signal from the gate **12G**. Transistor **12** is then cut-off, and this transistor presents a high impedance in the charging circuit. The bit line signal is terminated after the word line signal to insure that the capacitor **14** is nearly charged to the voltage on the bit line at the time transistor **12** is rendered nonconductive.

Thus, upon completion of the latter portion of the read-write cycle, a binary one or zero is written in each of the capacitors **14** in the first column of the memory and the voltage at the storage nodes **30** indicate whether a binary one or a binary zero is stored in the cell.

An alternate read-write scheme is depicted in FIG. 4B which differs for that shown in FIG. 4A in that the bit line voltage is normally maintained at a positive value and a negative pulse is applied to the bit line to reduce the voltage on the line to zero when it is desired to write a binary zero in a cell controlled by that bit line. In the practice of the invention using pulses of the type shown in FIG. 4B, a large signal provided by the discharge of capacitor **14** during read out indicates a binary zero, and a small signal indicates a binary one. During a write portion of read-write cycle, no signal is applied on top of the reference voltage of the bit line to write a binary one, and a negative signal is applied to write a binary zero.

Particular note should be made of the fact that in the array of FIG. 1 each storage cell requires only one field-effect transistor and one capacitor. Since the entire array can be fabricated on a single substrate using a well-known integrated circuit technique, each cell requires only a very small area on the substrate and, therefore, a very high cell density can be achieved. The memory itself is a destructive memory, by which it is meant that each read out operation destroys the information read out. That information must be rewritten in the memory if it is to be retained in storage. Further since the storage of the information is effected by the charge on the capacitors **14** and this type of storage is not permanent, it is necessary to periodically regenerate information stored in the memory. Various methods may be applied for regeneration. For example, every tenth cycle can be used to regenerate one of the word positions in the array with the other cycles being used for normal memory operations. In such a case the regenerating cycle would be applied in succession to the ward positions in the array. Regeneration can also be carried out by periodically reading out and rewriting all of the word positions in the array in sequence. The frequency with which regeneration operations must be performed is determined to a large degree by the size of the capacitor **14** and the leakage paths available for discharge of this capacitor when the connected transistor **12** is nonconducting. Leakage will be predominately through a reverse-biased semi-conductor junction and as such will be very sensitive to the temperature at that junction. Operation at temperatures in the order of 100° C. are possible and practical, but much greater storage times can be obtained if the temperature is reduced. Since the power dissipation in the cell can be quite low, in the order of one nanowatt or less during the static condition, it is relatively easy to maintain the array at a low temperature.

The entire memory array of the type shown in FIG. 1 in electrical form can be fabricated as an integrated circuit on a single silicon substrate. A preferred embodiment of one cell in such a substrate is illustrated in FIGS. 2 and 2A. The substrate is designated **32** and the entire surface of the substrate is covered with a thick layer of silicon dioxide **34** except at those places on the substrate where connections are to be made or devices constructed. The substrate **32** is P type and the source and drain for the cell (**12D** and **12S**) are formed by diffusing N type impurities through the surfaces of the substrate to form two N+ regions which are highly doped with this N type impurity. The two N+ regions, which serve as source and drain, are connected by a channel at the surface of the substrate. The word line **24** in FIG. 2 extends horizontally rather than vertically as in FIG. 1, and from this word line, which is a aluminum line deposited on the surface of the substrate, a tab extends over the region separating source **12S** and drain **12D** to form the gate electrode **12G**. The gate electrode **12G** is separated from surfaces of the wafer by a relatively thin layer of oxide **36**.

The source diffusion **12S** is actually a portion of a vertically extending diffusion, as viewed in FIG. 2 which forms both the source for each of the transistors in one row of the memory and also the bit line **26** for that row. Drain diffusion **12D** is a portion of a larger diffusion generally designated **38** in FIGS. 2 and 2A. This diffusion includes another retangular section, as viewed in FIG. 2, which is designated **14C** and forms one of the electrodes for the capacitor **14**. Immediately above the electrode formed by diffusion **14C** there is a thin layer of oxide **14B** which forms the dielectric for the capacitor. The second electrode is a deposited aluminum electrode **14A**. This upper electrode **14A** is connected to a metallized conductor **14D** on the surface of the substrate. This conductor is connected to the similar electrodes for the other capacitors **14** in the array and is terminated at a ground terminal, as is indicated in FIG. 1. The substrate itself is connected through a reference or biasing potential source **40** to ground. The entire substrate on which the memory is formed should be tied to a reference potential. Where, as here, the substrate is P type, a negative bias is conventionally employed for this purpose. Where an N type substrate is used, the substrate may be connected directly to ground.

Another embodiment of an integrated cell structure is shown in the sectional drawing of FIG. 3. This structure differs from that of the embodiment of FIGS. 2 and 2A in the manner in which the connection is made between the drain **12D** and the capacitor **14**. In the embodiment of FIG. 2 this connection is formed by the continuous diffusion **38** which includes both the drain portion **12D** of transistor **12**, and the electrode portion **14C** of capacitor **14**. In the embodiment of FIG. 3, in which wherever possible the same reference numbers are employed, the drain diffusion **12D** does not extend continuously to form one electrode of capacitor **14**. Rather a metallized connection is made at **42** to drain diffusion **12D** and this connection **42** is connected to the upper electrode **14A** of capacitor **14**. As before, a thin layer of oxide **14B** sparates electrodes **14A** from an N+ diffused layer **14C** which forms the other electrode for capacitor **14**. The ground connection to the capacitor **14** is made by a metallized conductor **44** which contacts diffused region **14C**.

Particular note should be made of the fact that in the embodiments of FIGS. 2, 2A and FIG. 3, the construction of the capacitor **14** is such as to avoid the connection in series with the capacitor of the capacitance which is normally present at a reverse biased junction in a field-effect device. Further connections are made directly to both electrodes of the capacitor and are not carried through the silicon substrate **32**. The electrode for the capacitor which is part of the silicon substrate is highly doped to be N+. The reason for this type of construction is to insure that any lower capacitances which are inherently present in the circuit are not in series with the capacitor **14** and, therefore, do not limit the establishing of a large charge on this capacitor. This structure has been found to be advantageous over those in which, for example, the capacitor is formed directly between an aluminum electrode and the P type substrate with a thin layer of oxide in between. With this type of construction the normal depletion layer at the surface of the P type substrate makes it difficult to achieve a large charge on the capacitor which does not leak off quickly.

Three further embodiments of the invention are shown in FIGS. 5, 6 and 7. Each of these embodiments is different from the embodiment of FIG. 1 primarily in that the capacitance, which is charged to store the information in each memory cell, is the gate to substrate capacitance of another field-effect transistor. The embodiments of these figures are advantageous in that integrated circuit memory cells are fabricated which require a minimum of components and which can be interrogated nondestructively. However, the capacitance of the field effect transistor which is used as the storage medium in each of these embodiments is not normally as large as the capacitance of the individual capacitor of FIG. 1, nor will it retain its charge for as long a time. Of course, the capacitance of the transistor can be increased by increasing the dimensions of the gate area. In each of the embodiments of FIGS. 5, 6 and 7 only the structure for a single cell is shown, it being realized that each of these cells is part of a larger array of the type that is shown in FIG. 1. Because of the fact that many of the lines and components perform the same functions and have the same structure in all the embodiments disclosed herein, wherever possible the reference numerals used in FIGS. 5, 6 and 7 correspond to those used in FIG. 1.

The memory cell of FIG. 5 requires only two field-effect transistors, the first of which is an input transistor **12** and the second of which is an output transistor **50**. Input transistor **12** has its gate **12G** connected to the appropriate word line **24** in the array and its source **12S** connected to the appropriate bit line. The drain **12D** of transistor **12** is connected to the gate **50G** of transistor **50**. The source **50S** of transistor **50** is connected to word line **24** and the drain **50D** of this transistor is connected to the bit line.

When it is desired to write a binary one in the memory cell, a positive voltage is applied, as indicated, to word line **24**. This voltage is applied both to the gate **12G** of transistor **12** and to the source **50S** of transistor **50**. If a binary one is to be written in the cell, a positive pulse is applied to bit line **26** and if a binary zero is to be written, this line is maintained at zero potential as is indicated in the drawing. Assuming a binary one is to be written and, therefore, a positive signal is applied to bit line **26**, this signal is applied to the source **12S** of transistor **12**, and to drain **50D** of transistor **50**. At this time the positive signal on word line **24** renders transistor **12** conductive so that the signal on the bit line **26** is transmitted through this transistor to gate **50G** of transistor **50**. Since at this time the source **50S** is at the high positive potential of the word line **24**, and the drain **50D** is at the positive potential of the bit line, the signal transmitted through transistor **12** to the gate **50G** of transistor **50** does not cause transistor **50** to conduct. For conduction in this device, which is again an NPN transistor, the gate voltage must be more

positive than the source voltage by an amount which is equal to the threshold voltage for the device. However, with transistor **12** conducting the gate capacitance of transistor **50** charges through transistor **12** towards the voltage value on bit line **26**. The word pulse on line **24** is terminated before the bit line pulse so that the charge is stored in transistor **50**. When during a write operation a zero is to be written and bit line **26** is maintained at zero, there is, of course, no charge stored in the transistor gate **50G**.

The information state of the cell of FIG. 5 is represented by the voltage at the node **30**. The voltage at this point is high when a charge is stored in the capacitance of transistor **50** indicating a binary one and the voltage at node **30** approaches ground when a zero is stored. The information stored is read out by holding the bit line at nearly zero potential and applying to word line **24** a negative signal, which is of opposite polarity to the signal applied during a write operation and has a different amplitude. The negative read signal applied to the gate **12G** is of the wrong polarity to cause conduction in transistor **12**, has no effect on this transistor, and thus does not disturb the information stored on node **30**. However, the negative signal applied to source **50S**, which is connected to the word line, allows conduction through transistor **50** if at this time a binary one is stored in node **30** and therefore gate **50G** is at a positive voltage. The word line signal is then passed through transistor **50** to the bit sense line to indicate that a one is still stored in the cell. If a zero is stored, gate **50G** is not sufficiently positive with respect to the source **50S** to allow transistor **50** to conduct and no pulse is produced on the bit line **26**. It should be noted that for best operation of the cell of FIG. 5, the threshold of device **50** should be comparable in magnitude to the voltage stored on node **30** in the one state and to the read pulse on the word line. With such a design, device **50** is not in a conductive state except when the read pulse on the word line is applied and when the one level is present on the node **30**. Otherwise cells which are not being read could "load down" the bit line and divert part of the sense signal during a read operation. Also terminals **12W** and **50W**, which are connected to the substrate on which the field-effect transistors are formed, should be biased to a negative value which is at least as negative as the read pulse applied to word line **24**. This prevents the junctions in transistor **50** from becoming forward biased during the read out operation.

The embodiment of FIG. 6 differs from that of FIG. 5 only in that a third field-effect transistor **52** has been added to the circuit. This transistor has its gate **52G** and its drain **52D** both connected directly to the node **30**, the voltage of which indicates whether a one or a zero is stored in the cell. The source **52S** of transistor **52** is connected to the bit line **26**. The function of transistor **52** is to make sure that the voltage at terminal **30** does not get too high. If the voltage at this terminal exceeds a predetermined value, the application of this voltage to the gate **52G** of transistor **52** causes this transistor to conduct until the voltage at node **30** has dropped to the proper value. The addition of transistor **52** to the circuit renders the electrical parameters of the circuit less critical. This, of course, is an important consideration in fabricating an integrated circuit type memory in which a large number of active devices are fabricated at a single time on one substrate and all must be operable within the design parameters of the circuit, if the board is to be used without the expense either of wiring in spare cells or using program interconnection techniques.

The embodiment of the memory cell shown in FIG. 7 is similar to that of FIGS. 5 and 6 in that only two field-effect transistors are required for each memory cell. This embodiment differs in that rather than a single word line and a single bit line being associated with each cell, there are two word lines **24W** and **24R** one of which is used to write and one of which is used to read. There are

also two bit lines 26W and 26R, which are respectively, a bit write line and a bit sense line. Through the use of the extra word and bit lines necessitates placing more conductors on the integrated circuit wafer, the embodiment of FIG. 7 is advantageous in removing design restraints which are present when bipolar signals must be applied to the same line. Further by this construction, the electrical parameters of the circuit are relaxed which both minimizes the possibility of errors during the operation and makes it easier to mass fabricate large members of operaable memory cells on a single wafer. As before, storage accomplished by charge on capacitance in the circuit which is primarily the gate to substrate capacitance of transistor 50. When a zero is stored in the cell, node 30 is at essentially zero voltge and when a one is stored, this node is at a positive voltage of, for example five volts. The write word line 24W is connected only to the gate 12G of transistor 12 and large positive signals are applied to this line during a write operation. The information to be written is determined by the voltage level on bit write line 26W which is connected only to the source 12S of the input transistor 12. This line is essentially at zero volts, if a zero is to be written and is raised by an appropriate signal to a voltage of about six volts when a one is to be written. The positive signal on the write word line, for example 12 volts, must be greater in amplitude than the positive signal on the bit line 26W by an amount which is at least equal to the threshold voltage which must ncessarily be applied to gate 12G of transistor 12 to cause this transistor to conduct. With a binary one representing signal on bit line 26W, conduction of transistor 12 charges the capacitance between the gate and substrate of transistor 50. This charge remains when the write signal on word line 24 is terminated, and then the bit signal on bit line 26W is terminated. The voltage at terminal 30 is then at about five volts. There is also capacitance in the reverse biased drain junction of transistor 12 which affects the charge stored and, therefore, the voltage at node 30.

During a read out operation a negative signal of about —5 volts is applied to read line 24R. If at this time the cell is storing a binary one and node 30 is at the higher positive voltage of between three and five volts, gate 50G is at a positive voltage which is in excess of the voltage of source terminal 50S by an amount in excess of the threshold for transistor 50. This transistor then conducts causing a signal to be delivered to the bit sense line 26R and this signal is transmitted to the sense amplifier connected to the line.

It should be apparent from the description above of the cell of FIG. 7 that if a signal is applied during a write operation to the bit write line 26W, the cell will be unaffected unless a signal is applied at that time to the write word line 24W. Similarly the cell is unaffected during a read operation unless a signal is applied to the read word line 24R.

It should also be noted that the features of the embodiment of FIG. 1 can be combined with those of FIG. 5. Thus a separate capacitor can be used to store the information representing charge and this charge can be coupled to the gate of a second transistor to allow nondestructive read out to be achieved.

As has been stated above, in each of the embodiments of the present invention, information is stored in the form of a charge on a capacitance in a storage cell. The charge is stored in either a separate capacitor or the capacitance included in one of the field-effect transistors in the cell. Tests have indicated that during worst-case conditions, leakage of this charge is sufficiently slow that regeneration is only necessary every 200 microseconds. Considering a 200 word array, read and write operations can be carried out in a hundred nanoseconds. Thus, all of the words in the memory can be successively regenerated in a period of 20 microseconds and memory operation can then be carried out for 180 microseconds (1800 read-write operations) before the next regeneration cycle. The regeneration need not be done at once but can be interspersed during a read-wire operation. In using the speeds and modes of operation described above only 10% of the total memory time is required for regeneration, and the effective read-write cycle time is less than 115 nanoseconds.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory; each said cell comprising:

(a) an input field-effect transistor including a channel between first and second regions to which first and second terminals for the transistor are connected, and including a gate electrode to which signals are applied to control the conduction between said terminals;

(b) a storage device exhibiting capacitance between first and second electrodes for the device and having a first one of said electrodes connected to said first terminal of said input field-effect transistor and its second electrode connected to a reference potential source;

(c) a word line for said cell connected to the gate electrode of said field-effect transistor;

(d) a bit line for said cell connected to the second terminal of said input field-effect transistor;

(e) and control means for controlling the writing of information in said cell comprising means for applying voltage signals to said word line and said bit line to cause said transistor to conduct and through said transistor to charge said capacitance of said storage device to a voltage representative of the information to be written in said cell;

(f) the voltage signal applied to said bit line being ineffective to change the information representing charge on said capacitance of said device in the absence of said signal applied to said word line to render said transistor conductive.

2. The memory of claim 1 wherein said control means includes means for controlling the reading out of information from said cell by applying a signal to said same word line used to control the writing of information in said cell.

3. The memory of claim 2 wherein said signal applied to said same word line during said read out of said cell is of a polarity opposite to that applied during said writing of information in said cell.

4. The memory of claim 3 wherein said storage device is another field-effect transistor having first and second terminals and a gate electrode for controlling conduction between said terminals, and which exhibits capacitance between its gate electrode and substrate, said first terminal of said input transistor being connected to the gate electrode of said another transistor, said word line being connected to the first terminal of said another transistor, and said bit line being connected to the second terminal of said another transistor.

5. The memory of claim 1 wherein each cell is coupled both to said word write line and to a separate word read line, and to said bit write line and to a separate bit read line.

6. The memory of claim 1 wherein said storage device for said cell is a capacitor.

7. The memory cell of claim 6 wherein each cell consists of only said input field-effect transistor and said capacitor.

8. The memory of claim 6 wherein said capacitor and said input field-effect transistor are formed at one surface of the same substrate and said first electrode of said capacitor is connected directly to said first terminal of said transistor and said second electrode of said capacitor is connected directly to a conductor to said reference potential at said same surface of said substrate.

9. The memory of claim 1 wherein said storage device for each cell is another field-effect transistor exhibiting capacitance between its gate electrode and substrate.

10. The memory cell of claim 9 wherein each said cell consists of only said input and said another field-effect transistors.

11. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory; each said cell comprising:

(a) an input field-effect transistor including a channel between first and second regions to which first and second terminals for the transistor are connected, and a gate electrode to which signals are applied to control the conduction between said terminals;

(b) a capacitor having first and second electrodes;

(c) said first terminal of said input transistor being connected to said first electrode of said capacitor;

(d) said second electrode of said capacitor being connected to a reference potential source;

(e) a word line connected to the gate electrode of said input transistor;

(f) a bit line connected to the second terminal of said input transistor;

(g) and means for writing information in said cell by applying signals to said word and bit lines to charge said capacitor through said input transistor, and for reading out information stored by applying a signal to said word line to discharge said capacitor through said input transistor to the voltage of said bit line.

12. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory; each said cell comprising:

(a) an input field-effect transistor and a capacitor;

(b) said word and bit lines being coupled to said input transistor to both write information in said cell by charging said capacitor through said transistor and to read information out of said cell by discharging said capacitor through said same transistor.

13. The memory of claim 12 wherein each of said cells includes only said input transistor and said capacitor and each said cell is coupled to only one word and one bit line in said memory.

14. The memory of claim 12 wherein said capacitor and said field-effect transistor are formed on one surface of the same substrate, a first one of the electrodes of the capacitor is connected at said surface to said field-effect transistor, and the other electrode of said capacitor is connected at said surface to a conductor connected to a source of reference potential.

15. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory; each said cell comprising:

(a) an input field-effect transistor and another field-effect transistor exhibiting capacitance between its gate electrode and the substrate of said another field-effect transistor;

(b) and each said cell being coupled to only one word line and one bit line in said memory and said input field-effect transistor being controlled to charge and discharge the capacitance of said another field-effect transistor through said input transistor to write information in said cell;

(c) said another field-effect transistor being nonconductive regardless of the charge stored therein in the absence of a signal on said word line;

(d) and said word line applying a signal to said another transistor to read out information from said cell.

16. The memory of claim 15 wherein each of said cells include a third field-effect transistor having its gate electrode and one of its terminals connected to the gate electrode of said another field-effect transistor and having its other terminal connected to said bit line for said cell.

17. The memory of claim 15 wherein each of said transistors includes source and drain terminals and a gate electrode, one of said terminals of said input transistor being connected to the gate electrode of said another transistor, and said word line being connected to the gate electrode of said input transistor and to one of the terminals of said another transistor.

18. The memory of claim 17 including means for applying a signal of one polarity to said word line to control writing in said cell and a signal of opposite polarity to control reading in said cell.

19. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory; each said cell comprising:

(a) an input transistor having first and second regions connected to first and second terminals for the transistor and a third region between said first and second regions coupled to a control terminal to which signals are applied for controlling current flow in either direction between said first and second terminals;

(b) a storage element exhibiting capacitance;

(c) said word and bit lines coupled to said transistor to write information in said cell by charging the capacitance of said storage element through said transistor to cause said cell to assume a first information representing state and to discharge the capacitance of said storage element through said transistor to cause said cell to assume a second information representing state.

20. The memory of claim 19 wherein said storage element is a capacitor having first and second electrodes, one of which is connected to said first terminal of said transistor, and wherein information stored in said capacitor is read out by discharging said capacitor through said transistor.

21. The memory of claim 19 wherein said input transistor is a field-effect transistor and said storage element is another field-effect transistor.

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TERRELL W. FEARS, *Primary Examiner.*

Exhibit 2

US005398205A

United States Patent [19]

Yamaguchi

[11] Patent Number: 5,398,205

[45] Date of Patent: Mar. 14, 1995

[54] **SEMICONDUCTOR MEMORY DEVICE HAVING TRENCH IN WHICH WORD LINE IS BURIED**

[75] Inventor: **Shinsuke Yamaguchi**, Tokyo, Japan

[73] Assignee: **NEC Corporation**, Tokyo, Japan

[21] Appl. No.: **239,555**

[22] Filed: **May 9, 1994**

[30] **Foreign Application Priority Data**

May 10, 1993 [JP] Japan 5-107852

[51] **Int. Cl.**[6] **G11C 11/34**; H01L 29/68

[52] **U.S. Cl.** **365/185**; 365/149; 257/301; 257/306; 257/309

[58] **Field of Search** 365/185, 149, 102; 257/296, 300, 301, 303, 306, 309, 622

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Primary Examiner—Eugene R. LaRoche
Assistant Examiner—Tan Nguyen
Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

[57] **ABSTRACT**

A semiconductor memory device including a plurality of memory cells of one-transistor and one-capacitor type is disclosed. Each of the memory cells includes a cell active region surrounded by a trench isolation region, a trench formed to cross the cell active region to thereby divide a surface portion of the cell active region into first and second parts, a word line formed in the trench in isolation form the cell active region by a gate insulating film, source and drain regions respectively formed in the first and second parts in contact with the trench, a first insulating film formed to cover the cell active region and the word line, a bit line formed in contact with a part of the drain region through a first contact hole provided in the first insulating film, a second insulating film formed to cover the bit line and the first insulating film, a storage electrode formed in contact with a part of the source region through a second contact hole provided in the first and second insulating films, a dielectric film formed on the storage electrode, and a cell plate electrode formed on the dielectric film.

5 Claims, 4 Drawing Sheets

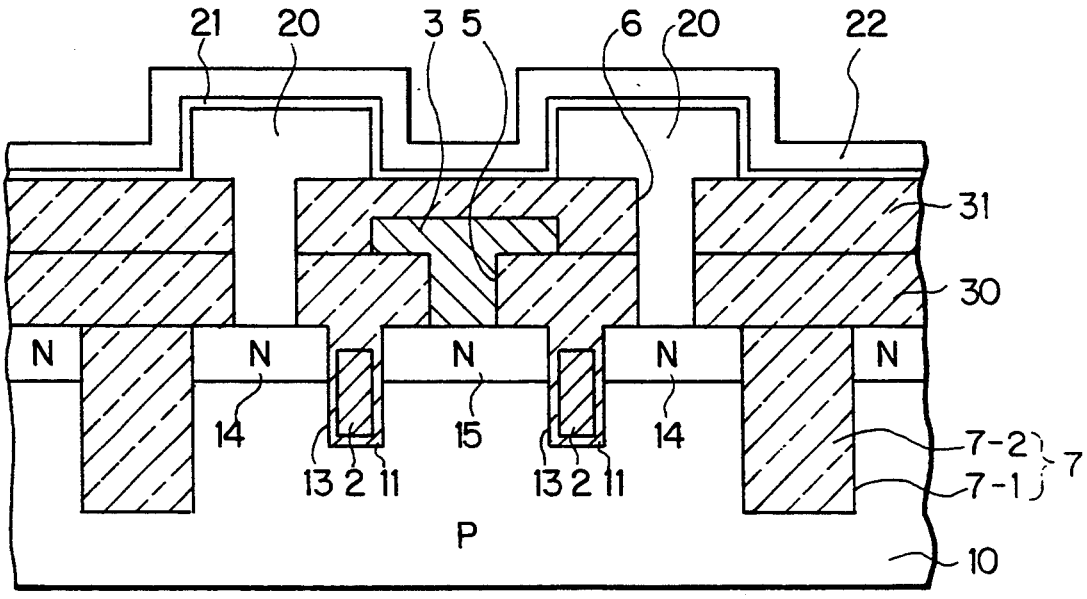


FIG. 1
PRIOR ART

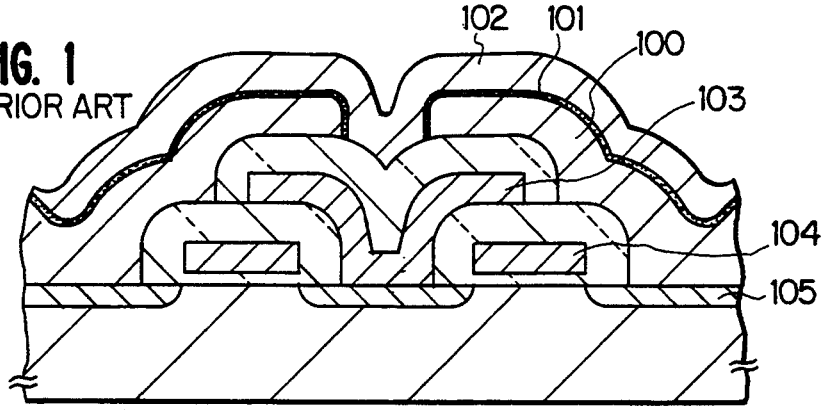


FIG. 2

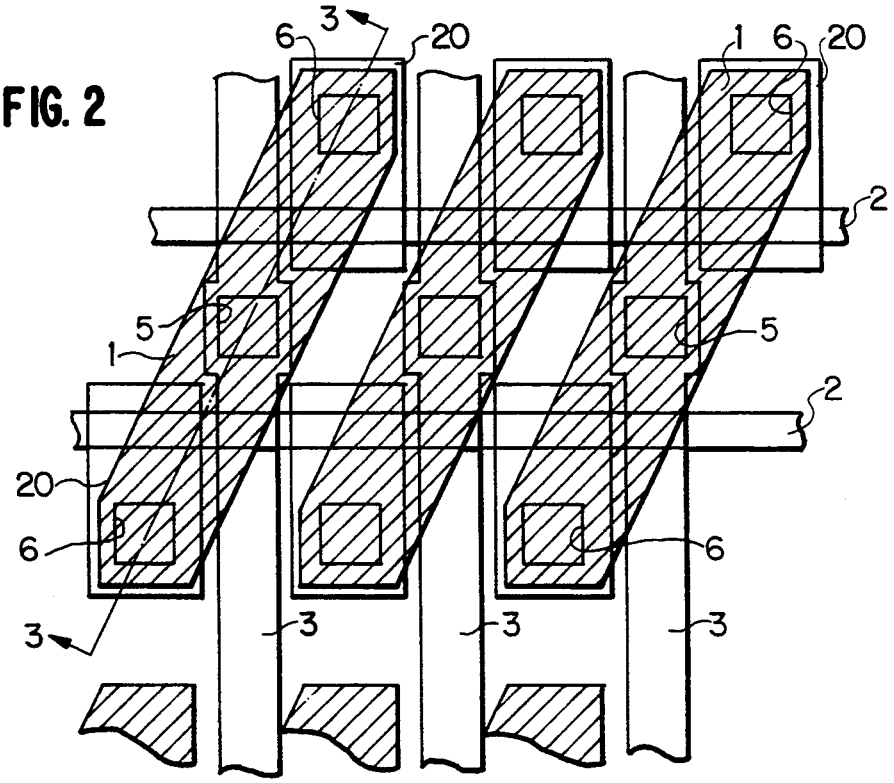


FIG. 3

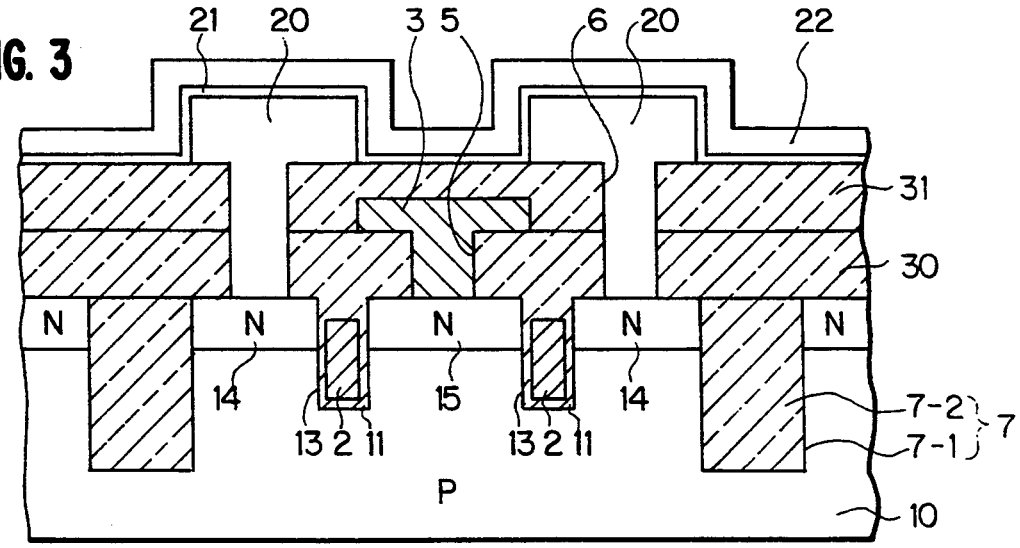


FIG. 4A

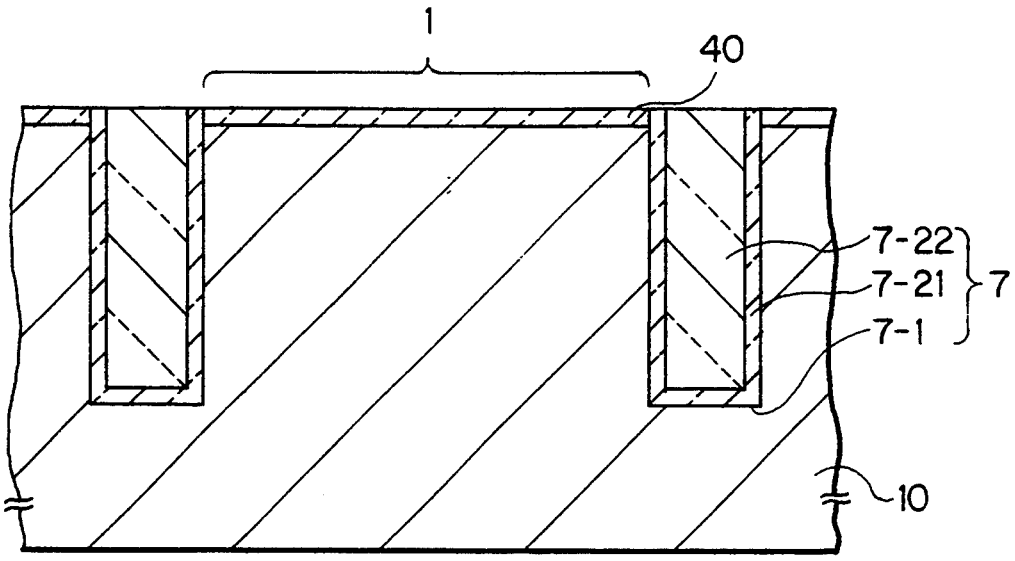


FIG. 4B

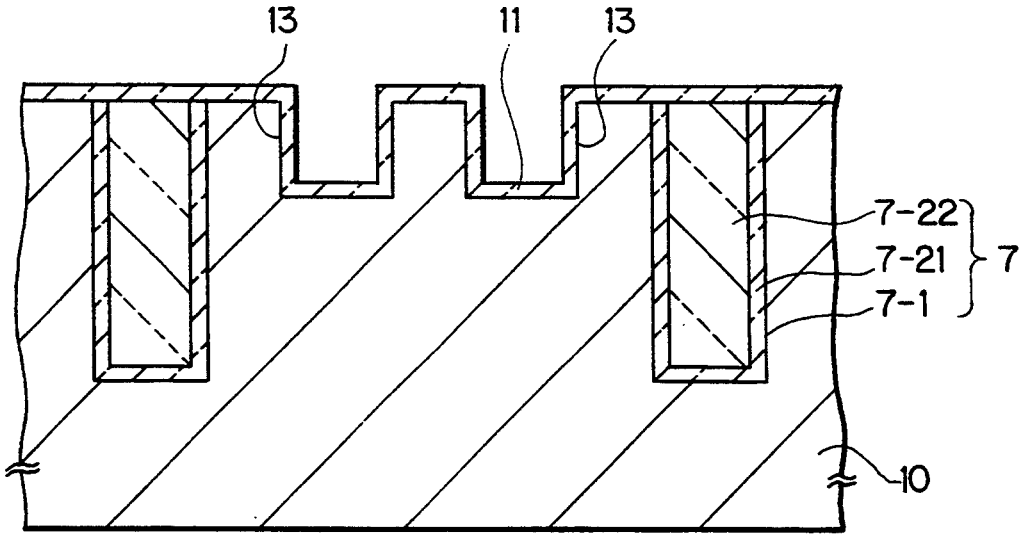


FIG. 4C

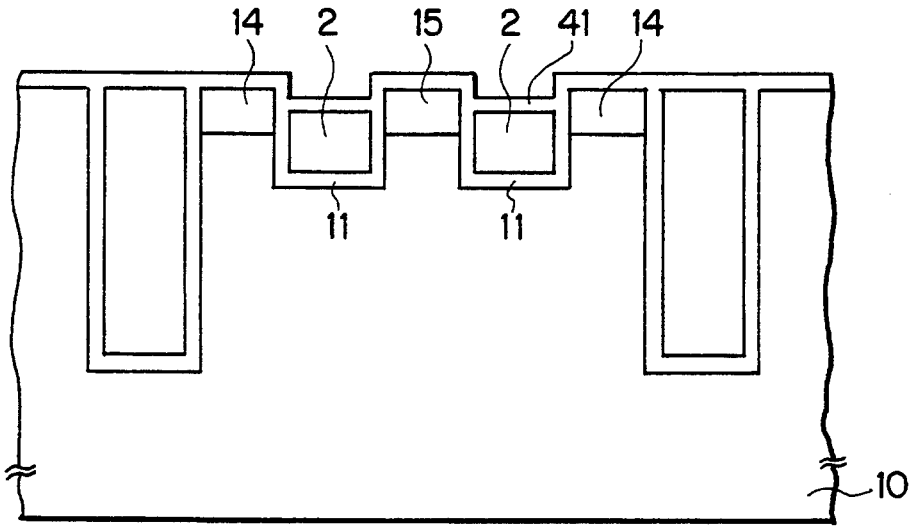
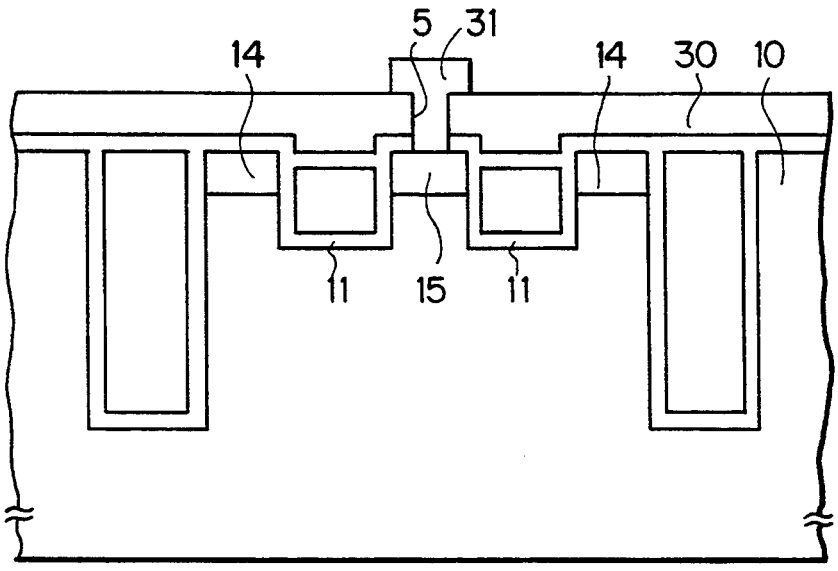


FIG. 4D



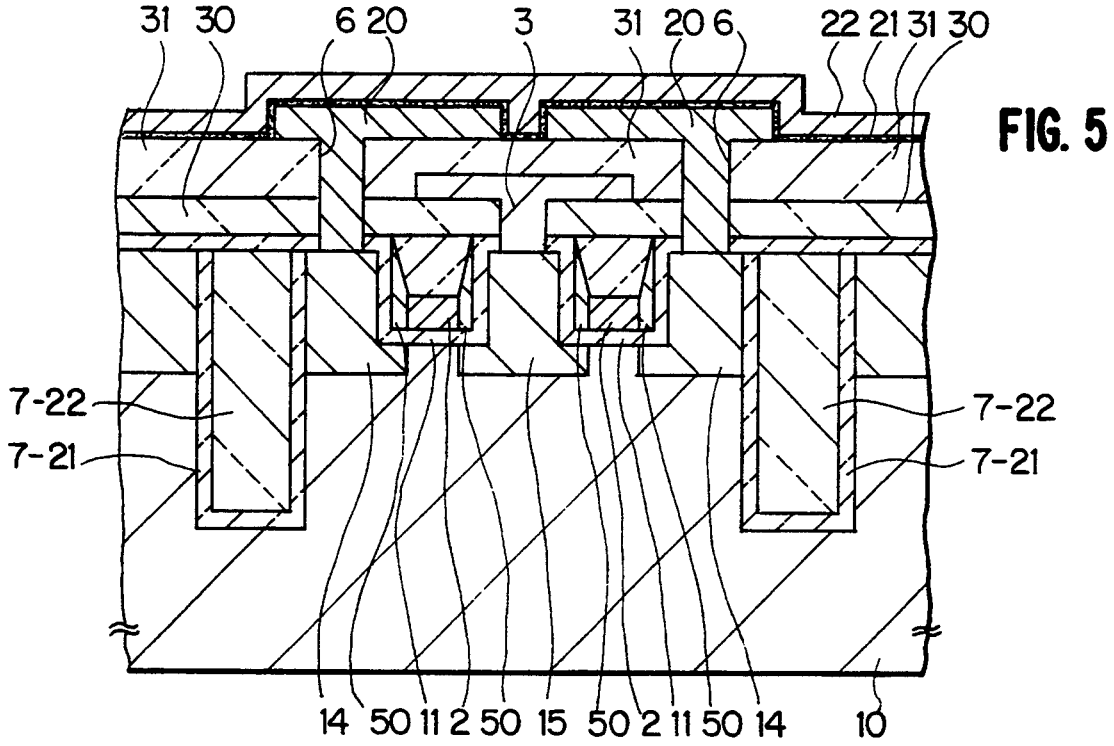
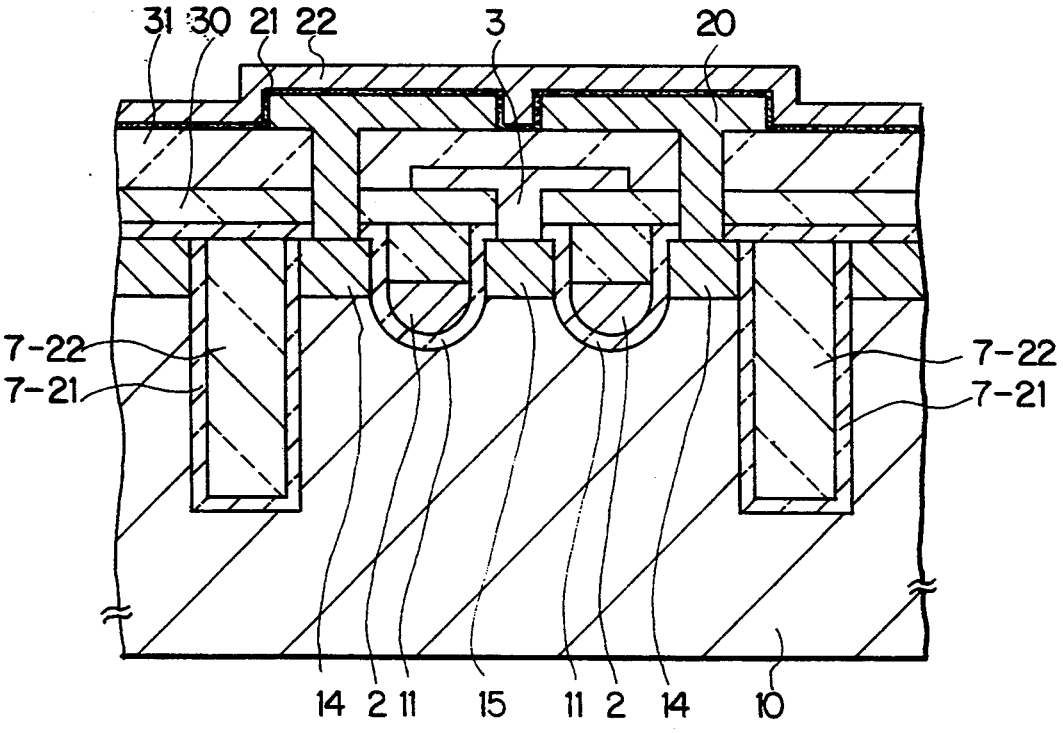

31 30 6 20 3 31 20 6 22 21 31 30
7-22
7-21
7-22
7-21
14 50 11 2 50 15 50 2 11 50 14 10

FIG. 5

FIG. 6


31 30 21 22 3 20
7-22
7-21
7-22
7-21
14 2 11 15 11 2 14 10

SEMICONDUCTOR MEMORY DEVICE HAVING TRENCH IN WHICH WORD LINE IS BURIED

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor memory device and, more particularly, to a dynamic random access memory device (DRAM) having memory cells each composed of one transistor and one storage capacitor.

In accordance with increase in memory capacity of a DRAM, an area which is able to be allotted to each memory cell, i.e. a cell size, is required be made small. The capacitance value of the storage capacitor is lowered accordingly. The decrease in capacitance value of the storage capacitor means that the amount of charges stored in the capacitor is made small, so that the data stored in each memory cell is easily destroyed.

In order to enhance the storage capacitance with a small cell size, therefore, a new stacked-type memory cell was proposed in "International Electron Devices Meeting Technical Digest", 1988, pp. 596–599, as titled "A New Stacked DRAM Cell Characterized by a storage Capacitor on a Bit-lone Structure". Referring to FIG. **1**, this proposed memory cell is characterized in that the storage electrode **100** of the capacitor is stacked over a bit line **103**. A dielectric film **101** is formed on the storage electrode **100**, and a cell plate electrode **102** is formed on the film **101**. Since the storage electrode **100** is formed over the bit line **103**, the surface area thereof is made enlarged, so that the relatively large storage capacitance is obtained. Incidentally, the reference numerals **104** and **105** denote a word line and a diffusion region such a source or a drain region, respectively.

In order to further enhance the storage capacitance, however, the storage electrode **100** has only to be made thick to thereby enlarge the side surface area thereof. As a result, the flatness of the device is deteriorated to make it difficult that wiring patterns for interconnecting respective circuit elements are made fine.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a semiconductor memory device having an improved memory cell structure.

It is another object of the present invention to provide a semiconductor memory device including memory cells each having an enlarged storage capacitance with a small cell size and with maintaining the flatness of the device.

A semiconductor memory device according to the present invention is characterized in that each of the memory cells formed in a semiconductor substrate includes a cell active region surrounded by a trench isolation region selectively formed in the semiconductor substrate, a trench formed to cross the cell active region to thereby divide a surface portion of the cell active region into first and second parts, an insulating film filling the trench, a word line buried in the insulating film, source and drain regions formed respectively in the first and second parts in contact with the trench, a first insulating layer formed to cover the source and drain regions and the insulating film and having a first contact hole to expose a part of the drain region, a bit line formed in contact with the part of the drain region through the first contact hole, a second insulating layer formed to cover the bit line and the first insulating layer, a second contact hole selectively formed in the first and second insulating layers to expose a part of the source region, a storage electrode formed in contact with the part of the source region through the second contact hole, a dielectric film formed on the storage electrode, and a cell plate electrode formed on the dielectric film.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings, wherein:

FIG. **1** is a cross sectional view illustrative of two memory cells according to the prior art;

FIG. **2** is a plan view illustrative of a part of a memory cell array according to a first embodiment of the present invention;

FIG. **3** is a cross sectional view along a line A–A' shown in FIG. **1**;

FIGS. **4A–4D** are cross sectional views indicative of manufacturing steps of the device shown in FIGS. **2** and **3**;

FIG. **5** is a cross sectional view illustrative of a second embodiment of the present invention; and

FIG. **6** is a cross sectional view illustrative of a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIGS. **2** and **3**, a semiconductor memory device according to a first embodiment of the present invention includes a plurality of cell active regions **1** arranged in a plurality of rows and columns. In this embodiment, two memory cells are formed in one cell active region **1**. Each of the cell active regions **1** are surrounded by a trench isolation region **7** and thus are isolated from one another. The trench isolation region **7** composed of a trench **7-1** selectively formed in a semiconductor substrate **10** made of silicon and an insulating material **7-2** such as a silicon dioxide film filling the trench **7-1**. The substrate **10** is of a P-type in the present embodiment. If desired, an N-type substrate can be employed.

Since two memory cells are formed in one cell active region **1**, two word lines **2** are formed to cross the cell active regions **1** arranged in one row. However, each of the word lines **2** is buried in the substrate **1** in isolation therefrom by a gate insulating film in accordance with the present invention. Specifically, a plurality of trenches **13** are selectively formed in each of the cell active regions **1** and the trench isolation region **7** to cross the associated one of the cell active regions **1**. Each of the trenches **13** are formed with the depth smaller than the trench **7** to thereby divide the surface portion of each cell active region **1** into three parts. Source regions **14** of an N-type are formed in two parts of the surface portion of the cell active region **1**, each of two parts being sandwiched the trenches **7** and **13**, and a drain region **15** of the N-type is formed in the remaining part sandwiched between the trenches **13**. Each trench **13** is covered with a gate insulating film **11**, and the associated one of the word lines **2** made of polysilicon is formed on the gate insulating film **11**. The top surface of each word line **1** is covered with a part of an insulating layer **30**. Thus, each word line **2** is buried in the substrate **10** in isolating therefrom by the gate insulating film **11**. Accordingly, the part of the substrate **10**

along the trench **13** between the source and drain region **14** and **15** serves as a channel region of a memory cell transistor, and a part of the word line **2** serves as a gate electrode thereof.

The substrate **10** having the memory cell transistor thus formed is covered with the insulating layer **30** such as silicon oxide. A plurality of bit line contact holes **5** are provided in the insulating layer **30** to expose respective parts of the drain regions **15**, and a plurality of bit lines **3** are formed on the insulating layer **30** and elongated in the direction of column. Each of the bit lines **3** is connected to the associated ones of the drain regions **15** through the bit line contact holes **5**. An insulating layer **31** such as a silicon oxide film is further formed to cover the insulating layer **30** and each bit line **3**.

A plurality of capacitor contact holes **6** are provided in the insulating layers **30** and **31** to expose respective parts of the source regions **14**. Formed through the contact holes **6** on the exposed part of the source region **14** is a storage electrode **20** made of polysilicon. This storage electrode **20** is elongated over the insulating layer **31** to enlarge the surface area thereof. A dielectric film **21** is formed over the entire surface of each storage electrode **20** and the insulating layer **31**, and a cell plate electrode **22** made of polysilicon is formed on the dielectric film **21**. Thus, a memory capacitor is formed to be connected to the b cell transistor.

As described above, each word line **2** is buried in the substrate **10**. The step over the surface of the substrate **10** is decreased accordingly. Therefore, even when the storage electrode **20** is made thick to further enlarge the surface area thereof, the surface flatness of the device is maintained.

The device illustrated in FIGS. **2** and **3** is produced in accordance with the steps shown FIGS. **4A** to **4D**. Specifically, as shown in FIG. **4A**, the P-type silicon substrate **10** is prepared and covered with s silicon dioxide film **40** and a mask layer (not shown). The dry-etching is then carried out to form the trench **7**. The cell active regions **1** are thereby defied by the trench **7**. The trench **7** is then covered by a silicon oxide film **7-21** and further filled with an insulating material **7-22** such as a silicon oxide film, a PSG film or a BPSG film. The trench isolation region **7** is thus formed.

As shown in FIG. **4B**, the oxide film **40** is removed and a new mask layer (not shown) is formed on the substrate **10**. The dry-etching is then performed to remove the respective parts of each cell active region **1** and the trench isolation region **7** to thereby form the trenches **13**. The heat treatment is then performed to form the gate oxide film **11** on the surface of each trench **13**.

As shown in FIG. **4C**, a polysilicon film is deposited over the entire surface and a selective-etching process is then carried out to form the,polysilicon word lines **2**. After covering the top surface of each word line **2** with a silicon oxide film **41**, impurity ions indicative of the N-type such as arsenic or phosphorus are implanted into the parts of the substrate **10** and the word lines **2**, followed by the heat treatment to activate the ion-implanted impurities. The source and drain regions **14** and **15** are thereby formed and each word line **2** is lowered in the resistance thereof.

As shown in FIG. **4D**, the insulating layer **30** such a silicon oxide film is formed on the entire surface, and the bit line contact holes **5** are selectively formed in the insulating layer **31**. The bit lines **3** made of silicide of silicon and a refractory metal is formed in contact with the associated ones of the drain regions **15** through the bit line contact holes **5**.

Thereafter, as shown in FIG. **3**, the insulating layer **31** is deposited over the entire surface and the capacitor contact holes **5** are formed to expose the respective parts of the source regions **14**. The cell capacitors are thereafter formed as mentioned above.

Referring to FIG. **5**, there is shown a device according to a second embodiment of the present invention, in which the same constituents as those shown in FIGS. **2–4** are denoted by the same reference numerals to omit the further description thereof. In this embodiment, a silicon oxide film **50** is formed along each side surface of the respective word lines **2**. This oxide film **2** prevents the concentration of the electric field applied to the respective corner portions of each trench **13**, so that the gate oxide film **11** is protected from the destruction. Further in this embodiment, each of the source and drain regions **14** and **15** is formed deeper to define the channel region of the cell transistor at the bottom portion of the trench **13**.

Turning now to FIG. **6**, the memory cell shown therein has the trenches **13** each formed with a rounded bottom in accordance with a third embodiment of the present invention. The other constituents are the same as those shown in FIGS. **2–4**. Accordingly, the gate oxide film **11** is protected from the destruction without forming the oxide film **50** shown in FIG. **5**.

It is apparent that the present invention is not limited to the above embodiments, but may be modified and changed without departing from the scope and spirit of the invention. For example, the respective conductivity types are changed to other types, and the other suitable impurities can be employed to form the source and drain regions. Moreover, the material for the respective insulating films or layers may replaced with other suitable ones. Furthermore, the source and drain regions may be formed before forming the word lines.

What is claimed is:

1. A semiconductor memory device having a plurality of memory cells formed in a semiconductor substrate of one conductivity type, each of said memory cells comprising a cell active region surrounded by a trench isolation region selectively formed in said semiconductor substrate, a trench formed to cross said cell active region to thereby divide a surface portion of said cell active region into first and second parts, a word line formed in said trench in isolation from said cell active region by a gate insulating film, first and second regions of an opposite conductivity type respectively formed in said first and second parts of said surface portion of said cell active region in contact with said trench, a first insulating layer formed to cover said word line and said cell active region, a first contact hole selectively formed in said first insulating layer to expose a part of said first region, a bit line formed in contact with said part of said first region through said first contact hole, a second insulating layer formed to cover said bit line and said first insulating layer, a second contact hole selectively formed in said first and second insulating layers to expose a part of said second region, a storage electrode formed in contact with said part of said second region, a dielectric film formed on said storage electrode, and a cell plate electrode formed on said dielectric film.

2. The device as claimed in claim **1**, wherein said trench has a bottom portion and a side portion, said gate insulating film having a first portion formed on said bottom portion of said trench with a first thickness and

a second portion formed on said side portion of said trench with a second thickness that is lager than said first thickness.

3. The device as claimed in claim 1, wherein said trench has a bottom portion, each of said first and second regions terminating at said bottom portion of said trench to define a channel region along a part of said bottom portion of said trench.

4. The device as claimed in claim 1, wherein said trench has a rounded bottom portion to be free from formation of an edge corner.

5. A semiconductor memory device comprising a semiconductor substrate of one conductivity type, a first trench formed in said semiconductor substrate in a mesh shape to define a plurality of cell active regions in said semiconductor substrate, said cell active regions being thereby arranged in a plurality of rows and columns, a first insulating film filling said first trench, a plurality of second trenches each provided correspondingly to each of said rows, each of said second trenches thereby crossing associated ones of said cell active regions arranged in the same row to divide a surface portion of each of the associated ones of said cell active regions into first and second parts, a plurality of word lines each formed in each of said second trenches in isolation from each cell active region by a gate insulating film, a plurality first regions of an opposite conductivity type each formed in an associated one of said first parts of said surface portions of said cell active regions, a plurality of second regions of said opposite conductivity type each formed in an associated one of said second parts of said surface portion of said cell active regions, a second insulating film formed to cover said cell active regions and said first insulating film, a plurality of first contact holes formed in said second insulating ,film to expose respective parts of said first regions, a plurality of bit lines each provided correspondingly to each of said columns, each of said bit lines being thereby in contact through said first contact holes with each of said parts of said first regions arranged in the same column, a third insulating film formed to cover said second insulating film and said bit lines, a plurality of second contact holes formed in said second and third insulating films to expose respective parts of said second regions, a plurality of storage electrodes each formed in contact with an associated one of said parts of said second regions, a dielectric film formed to cover each of said storage electrodes and said third insulating film, and a cell plate electrode formed on said dielectric film.

* * * * *

Exhibit 3

US008048737B2

(12) **United States Patent**
Kim et al.

(10) **Patent No.: US 8,048,737 B2**
(45) **Date of Patent: Nov. 1, 2011**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME**

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(73) Assignee: **Hynix Semiconductor, Inc.**, Icheon (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 74 days.

(21) Appl. No.: **12/648,710**

(22) Filed: **Dec. 29, 2009**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
H01L 27/108 (2006.01)

(52) **U.S. Cl.** **438/253**; 257/302; 257/E27.091; 257/E21.646

(58) **Field of Classification Search** 438/253; 257/302
See application file for complete search history.

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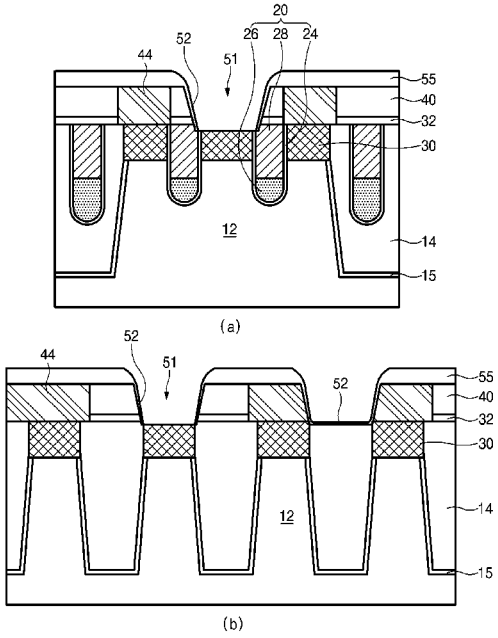
Primary Examiner — A. Sefer

(57) **ABSTRACT**

The invention relates to a semiconductor device and a method of fabricating the same, wherein a storage node contact hole is made large to solve any problem caused during etching a storage node contact hole with a small CD, a landing plug is formed to lower plug resistance, and the SAC process is eliminated at the time of the bit line formation. A method of fabricating a semiconductor device according to the invention comprises: forming a device isolation film for defining a multiplicity of active regions in a semiconductor substrate; forming a multiplicity of buried word lines in the semiconductor substrate; forming a storage node contact hole for exposing a storage node contact region of two adjoining active regions; filling the storage node contact hole with a storage node contact plug material; forming a bit-line groove for exposing a bit-line contact region of the active region and splitting the storage node contact plug material into two; and burying the bit line into the bit-line groove.

11 Claims, 13 Drawing Sheets



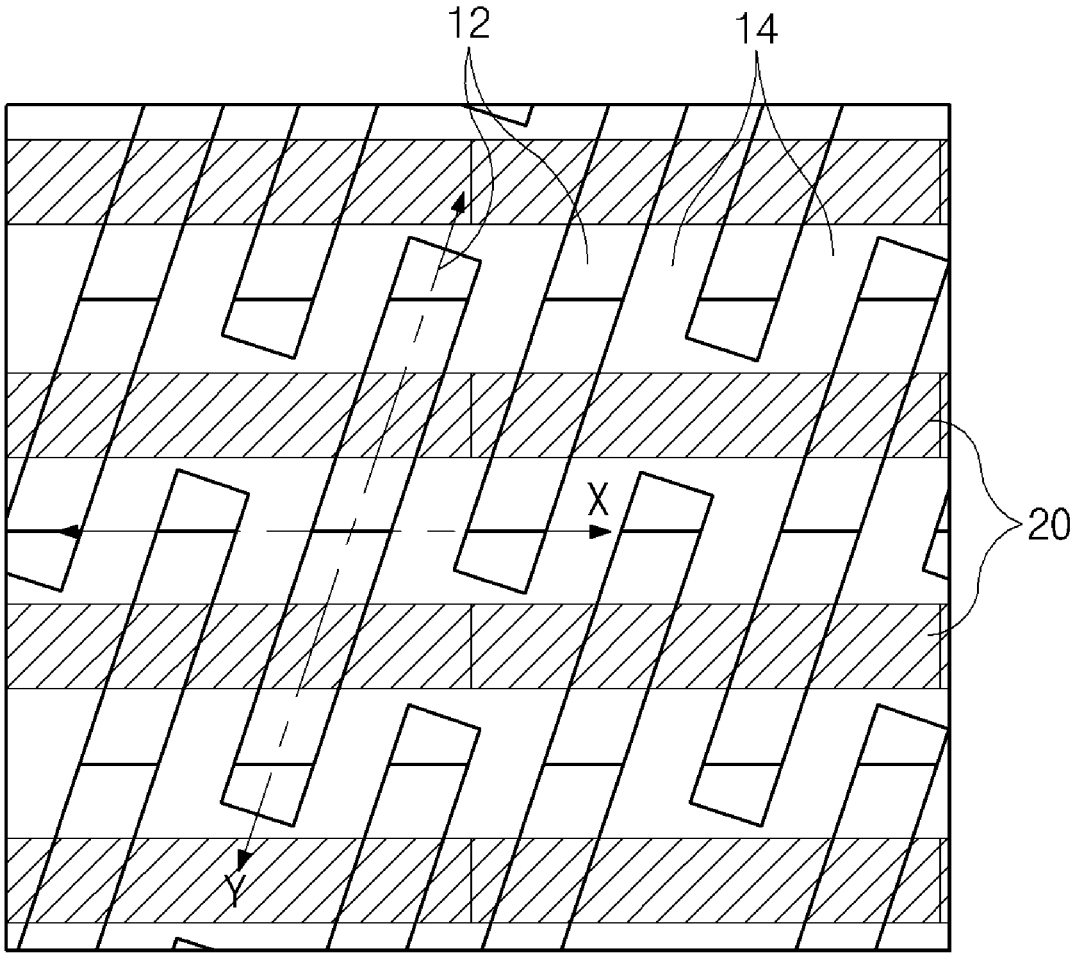
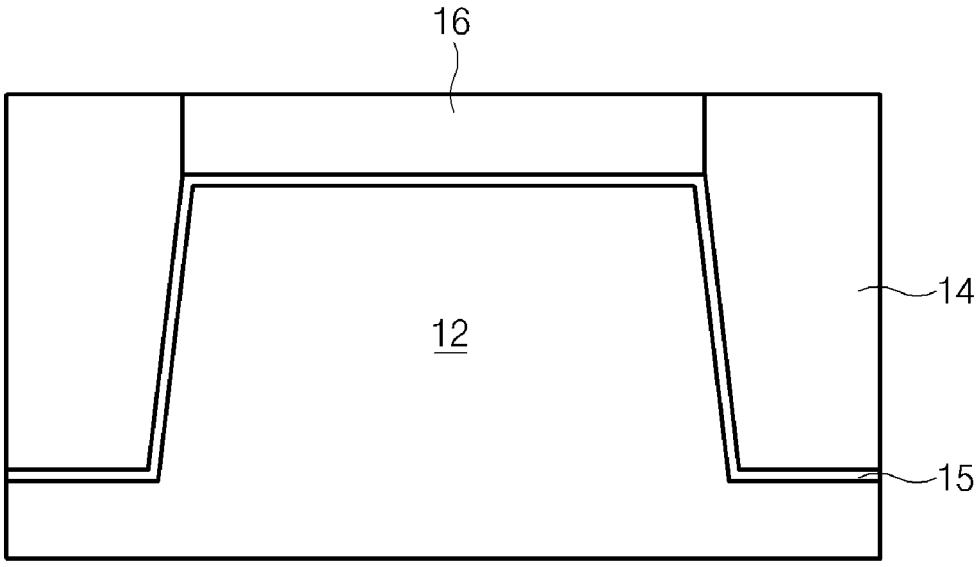


Fig.1



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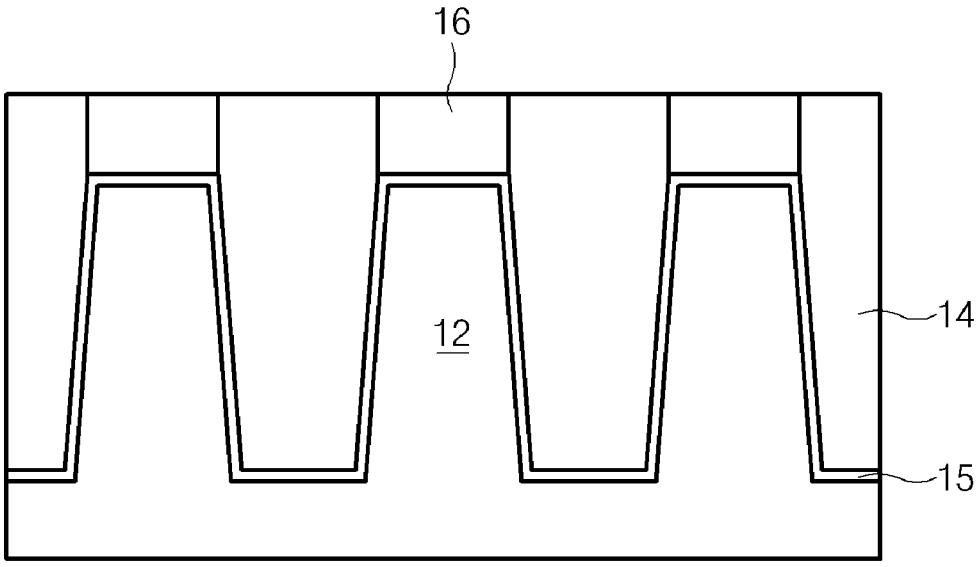
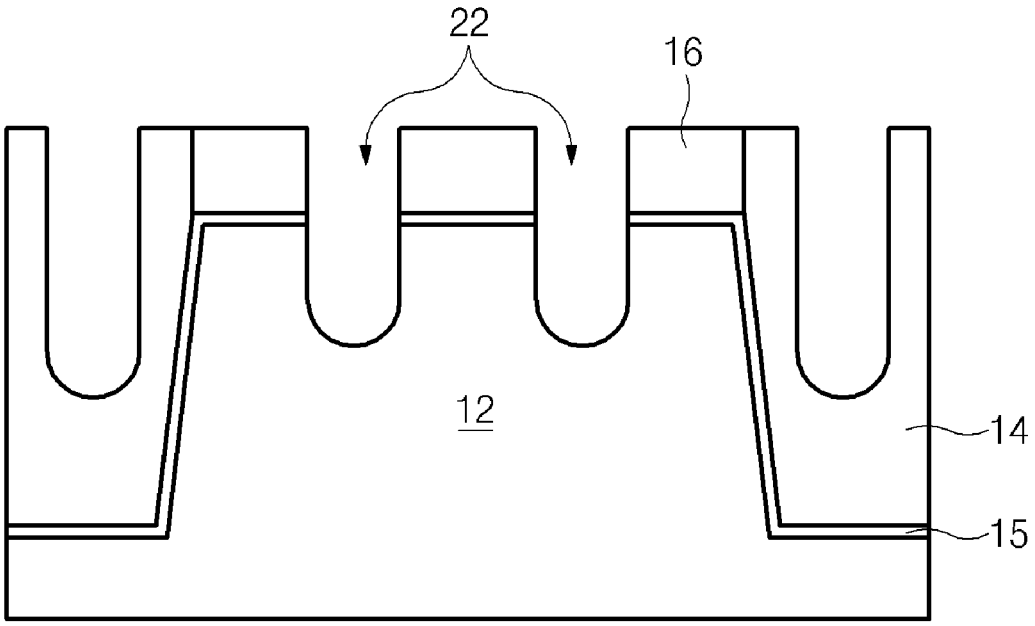


(b)

Fig.2



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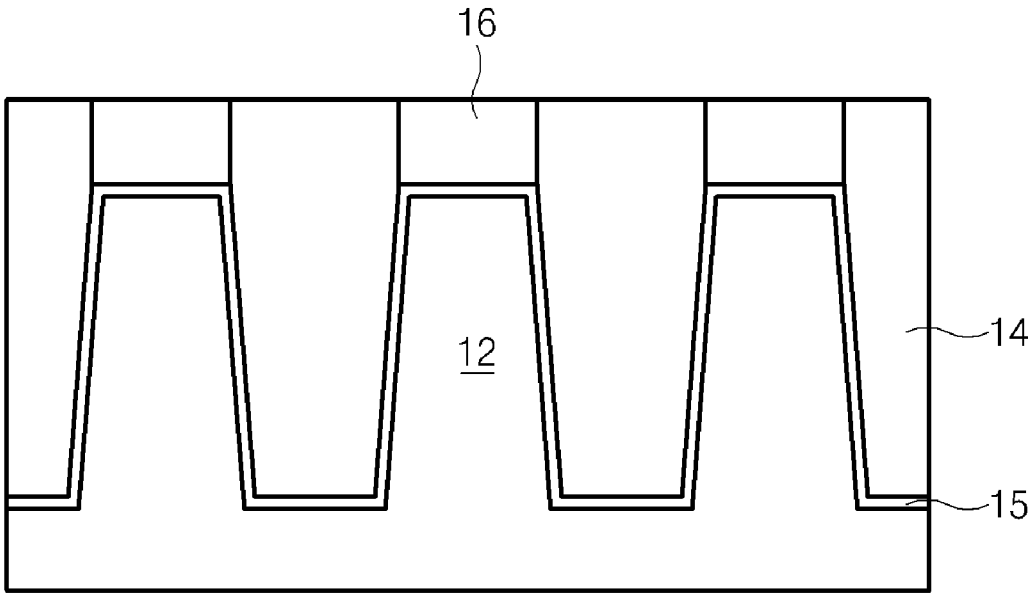
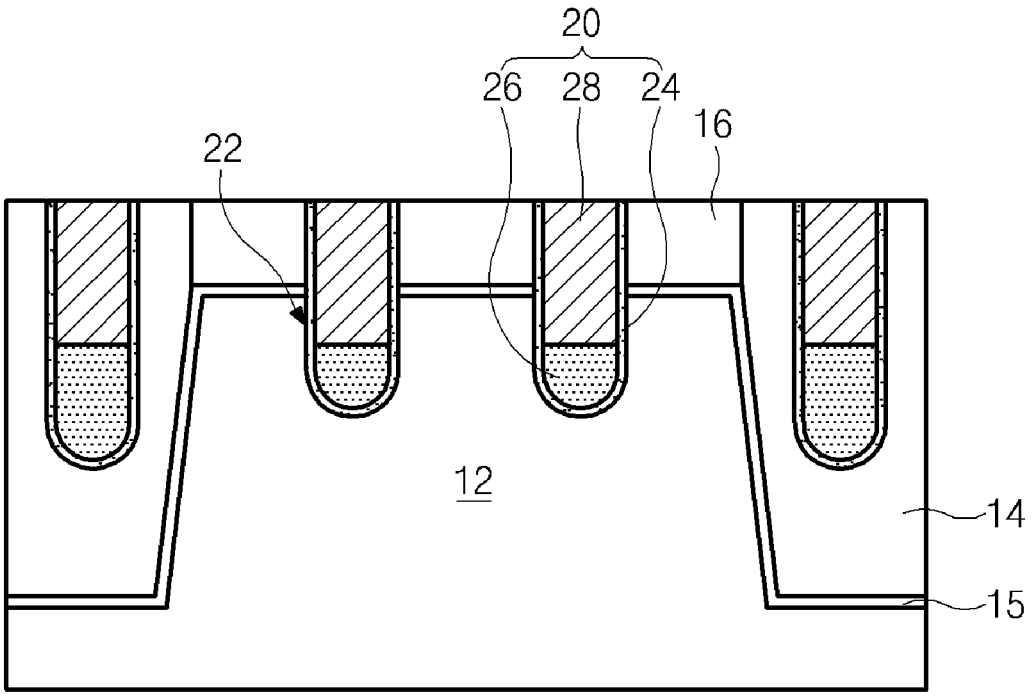


(b)

Fig.3



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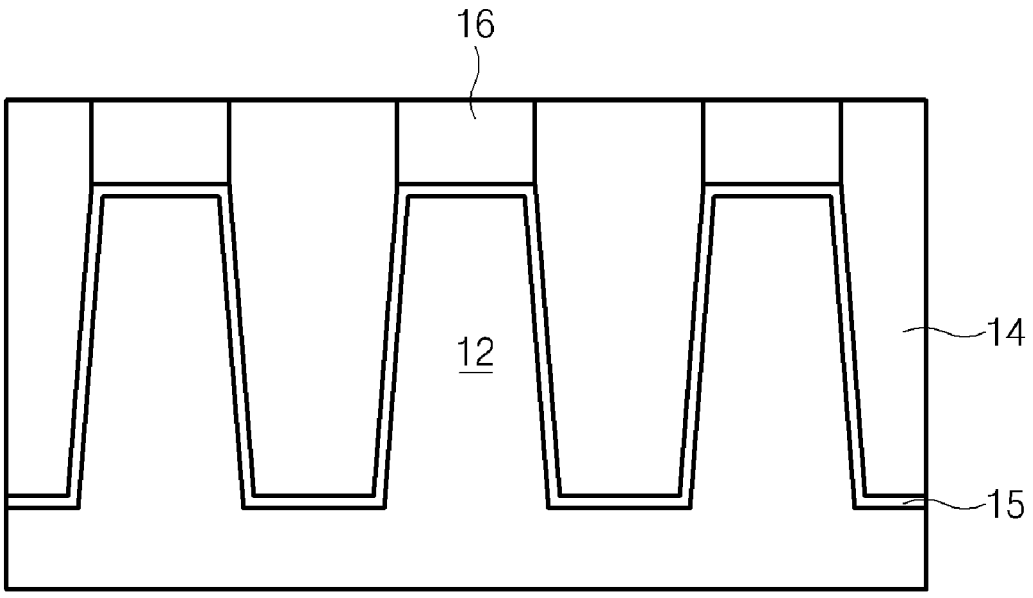
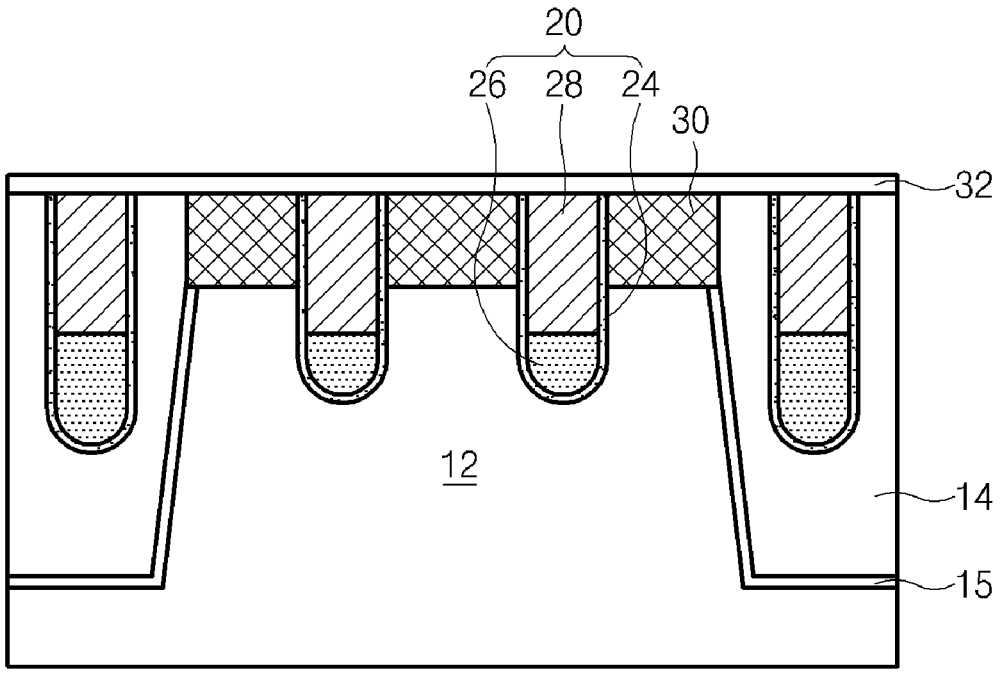


(b)

Fig.4



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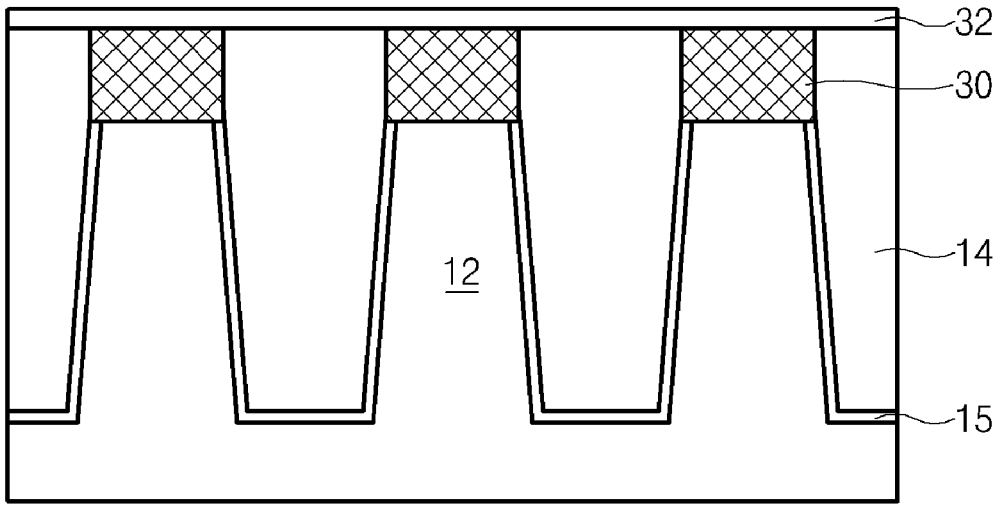

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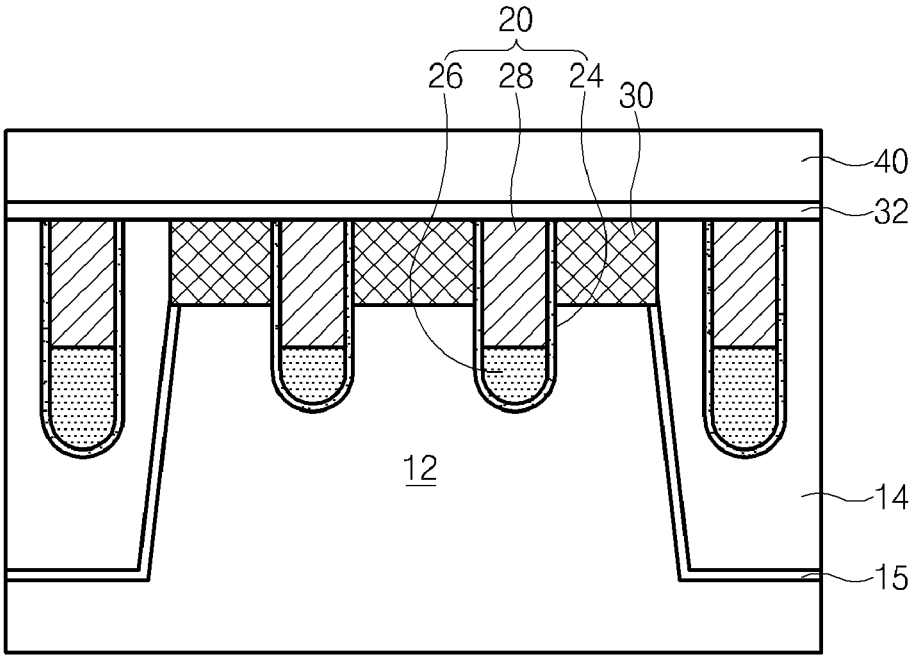
Fig.5



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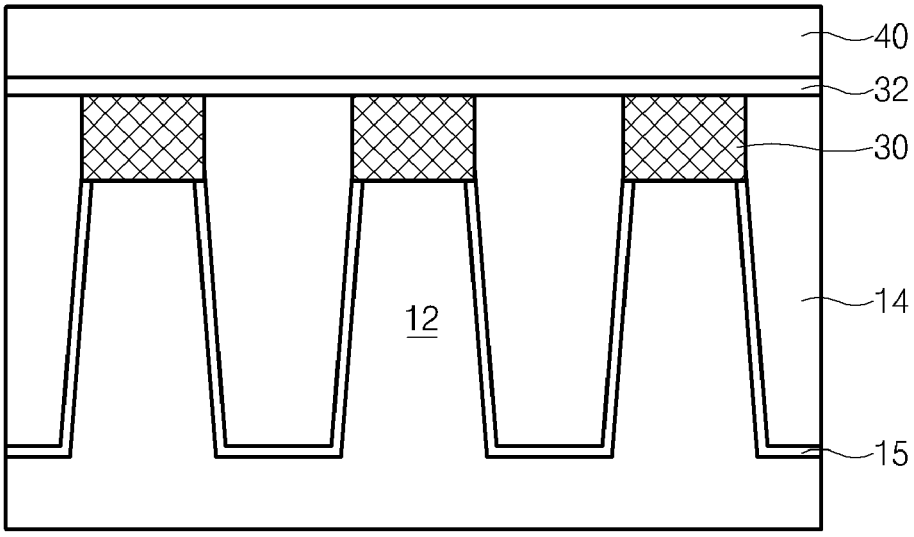

(b)

Fig.6

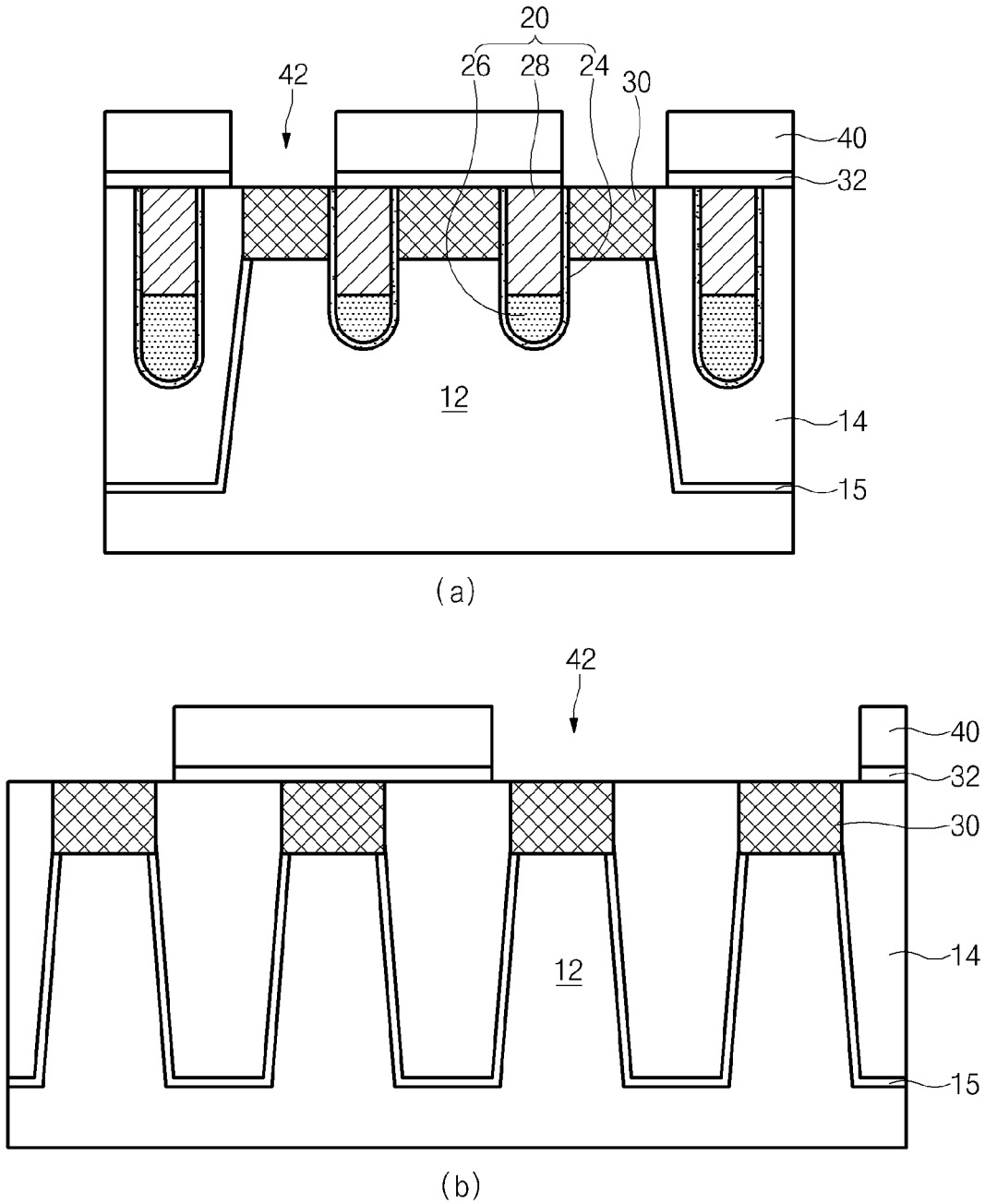

Fig.7

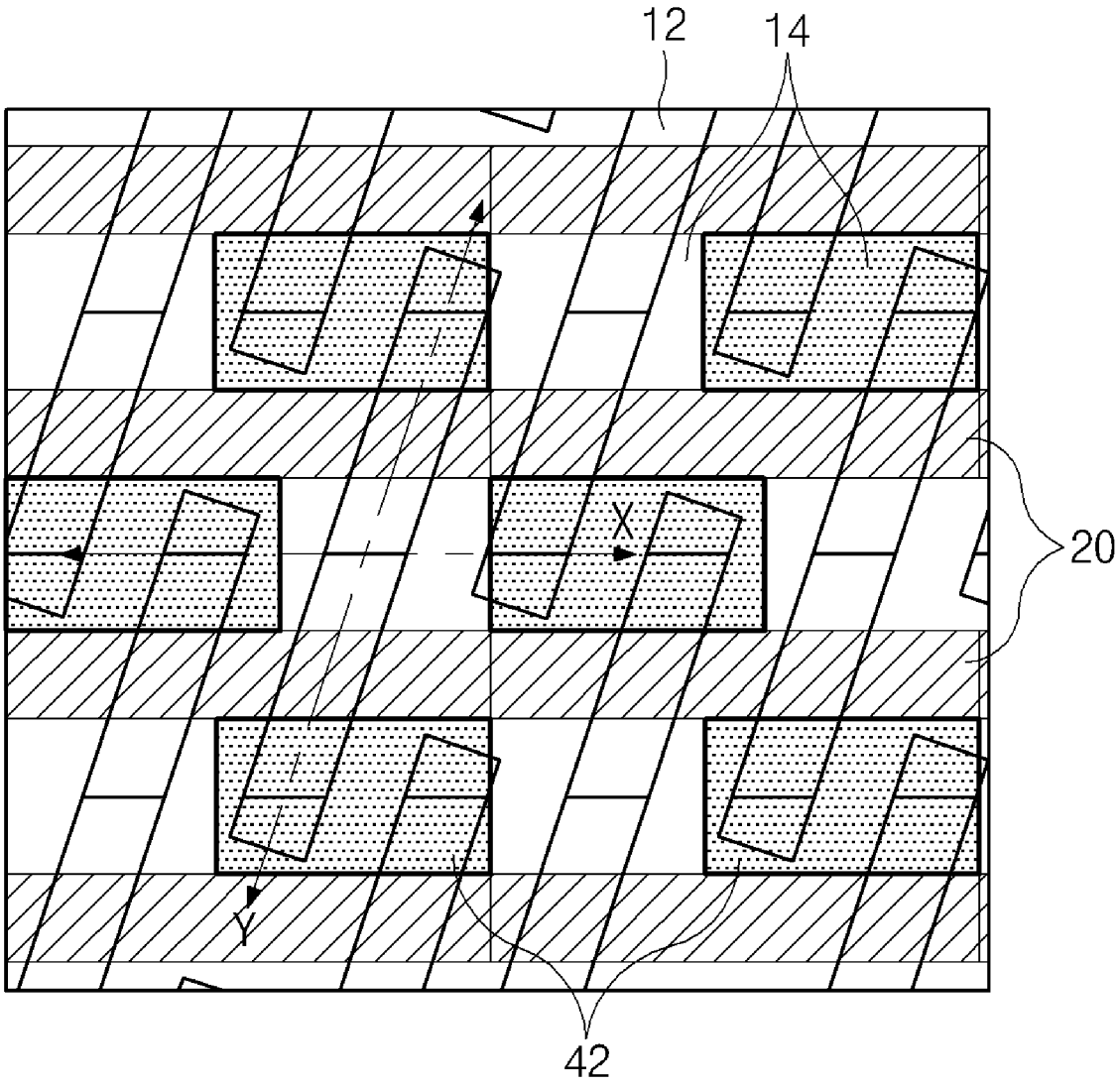

Fig.8

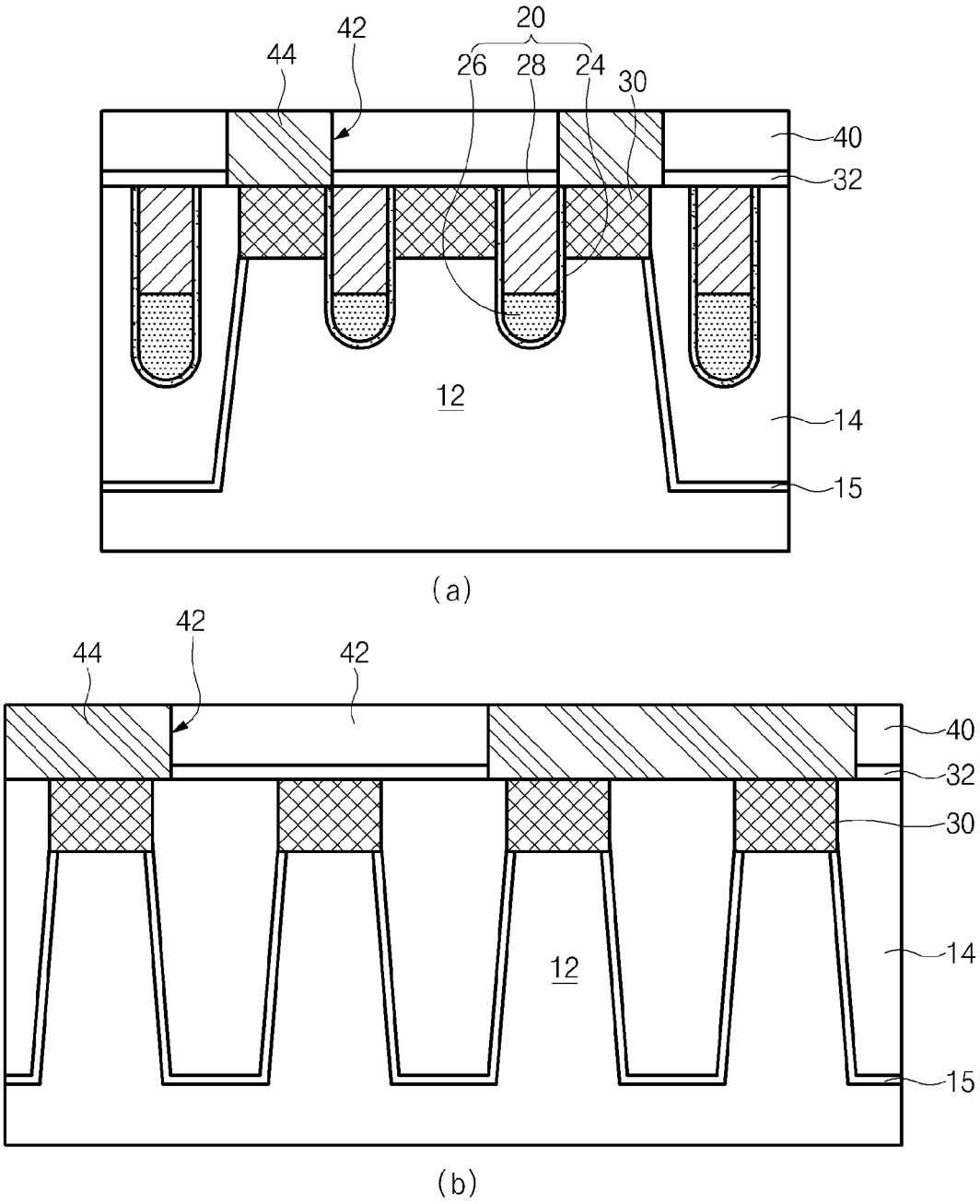

Fig.9

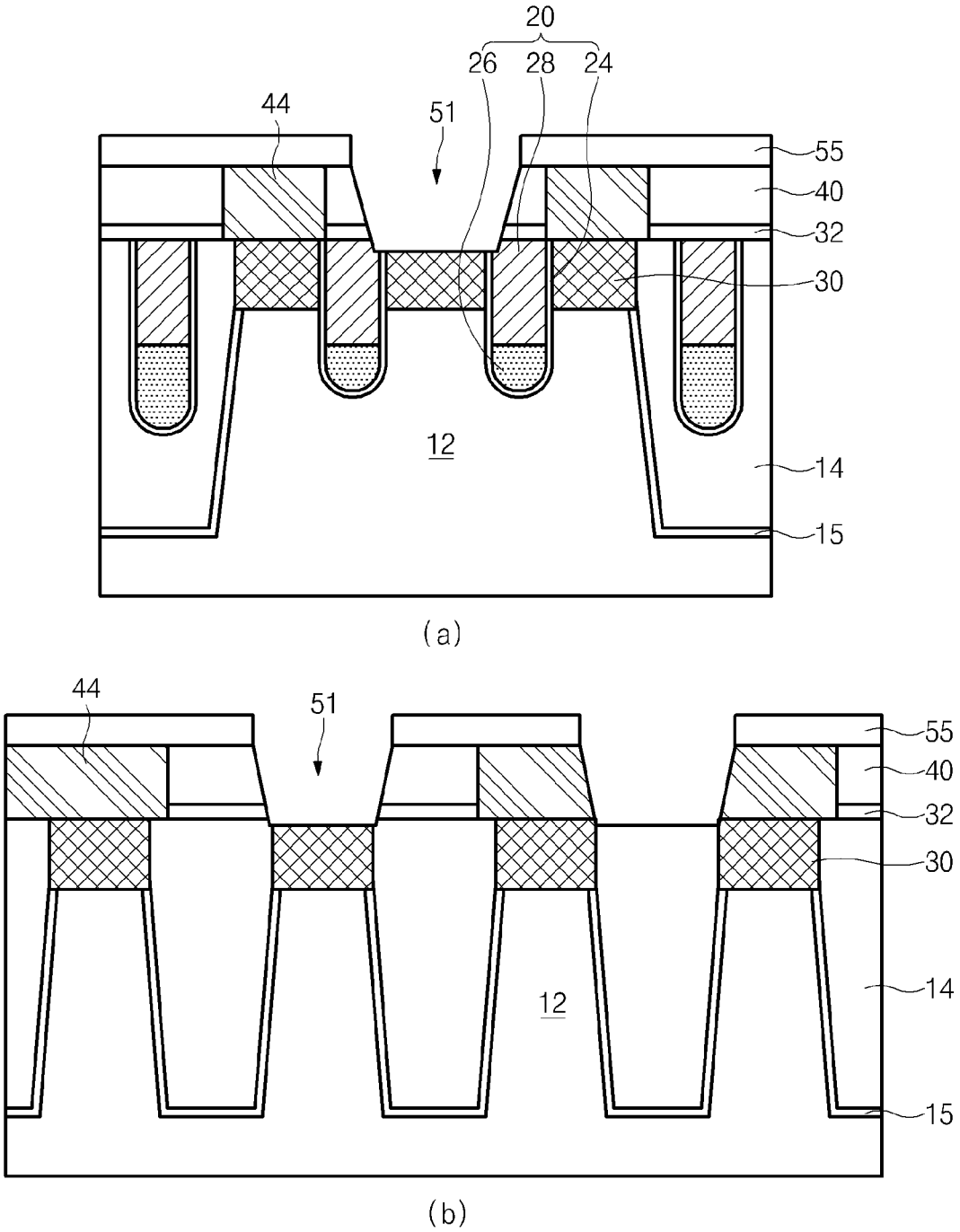

Fig.10

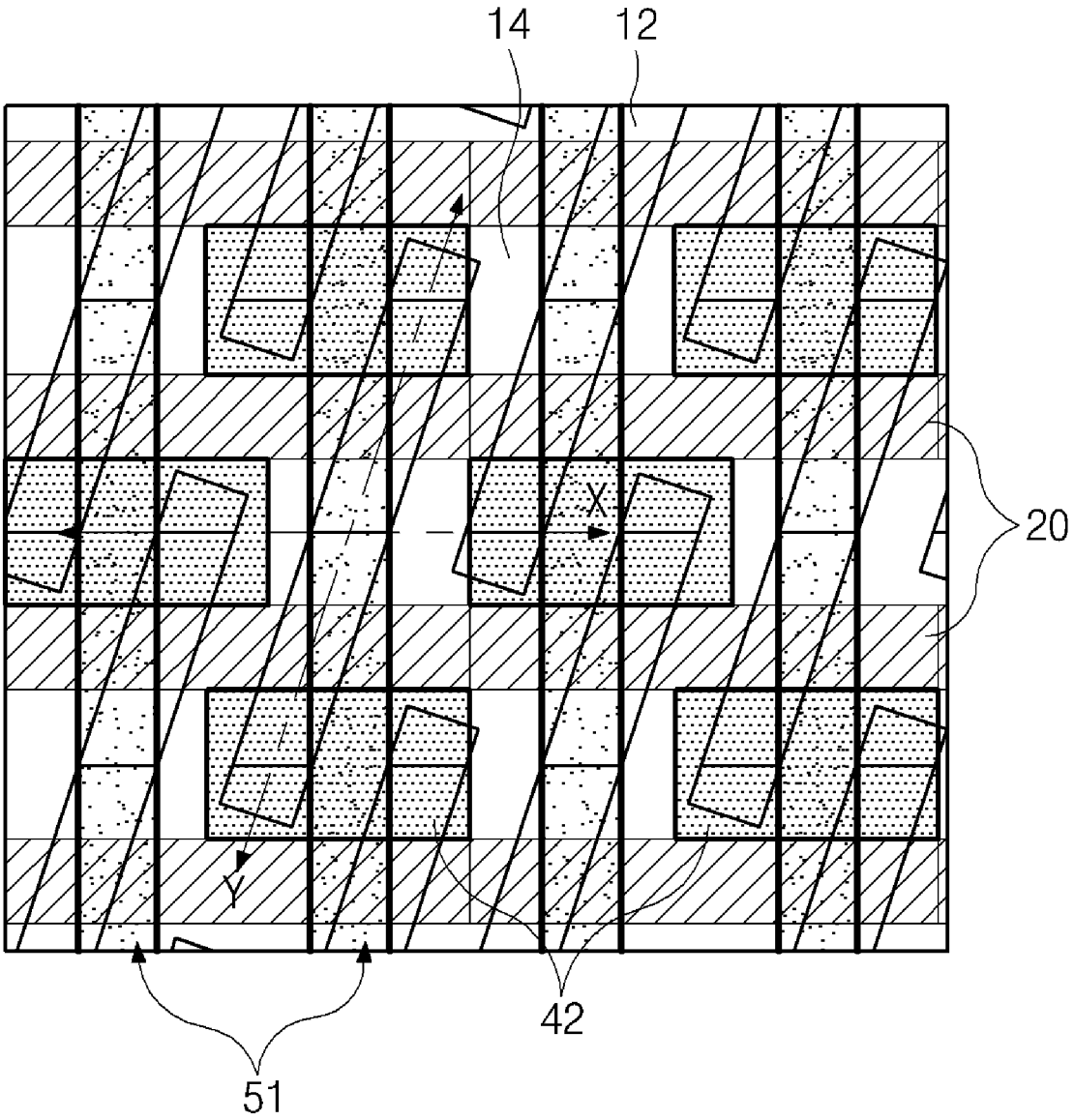

Fig.11

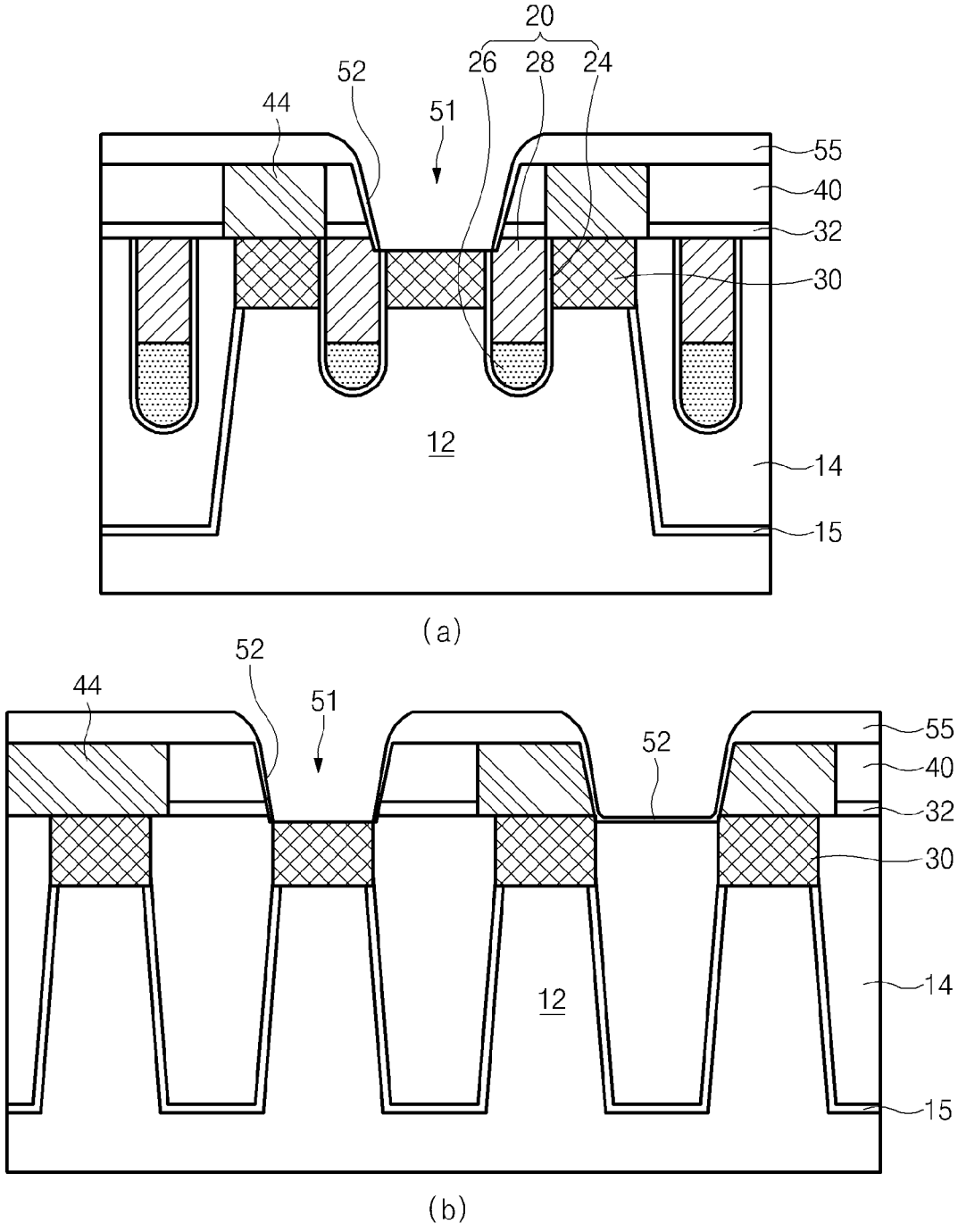
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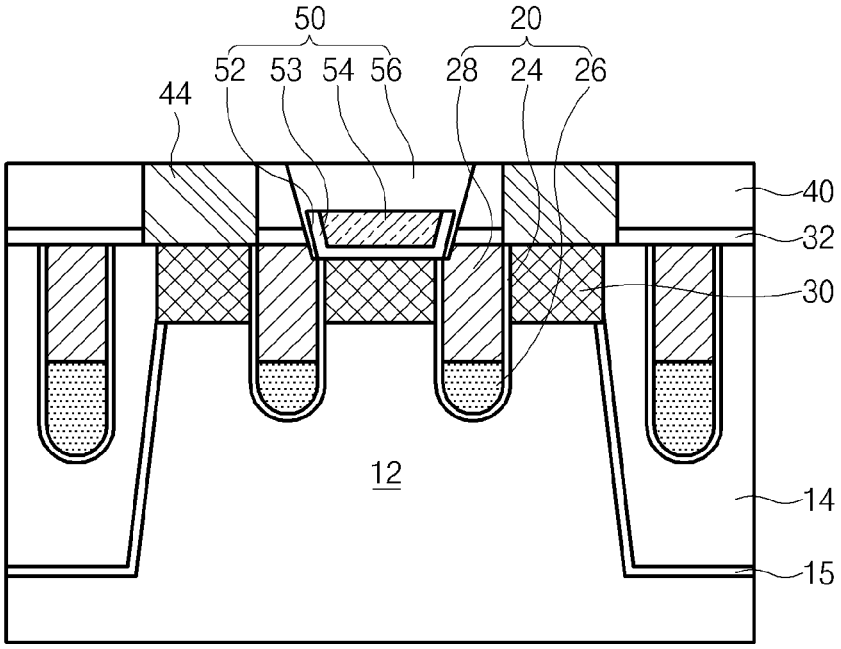
Fig.12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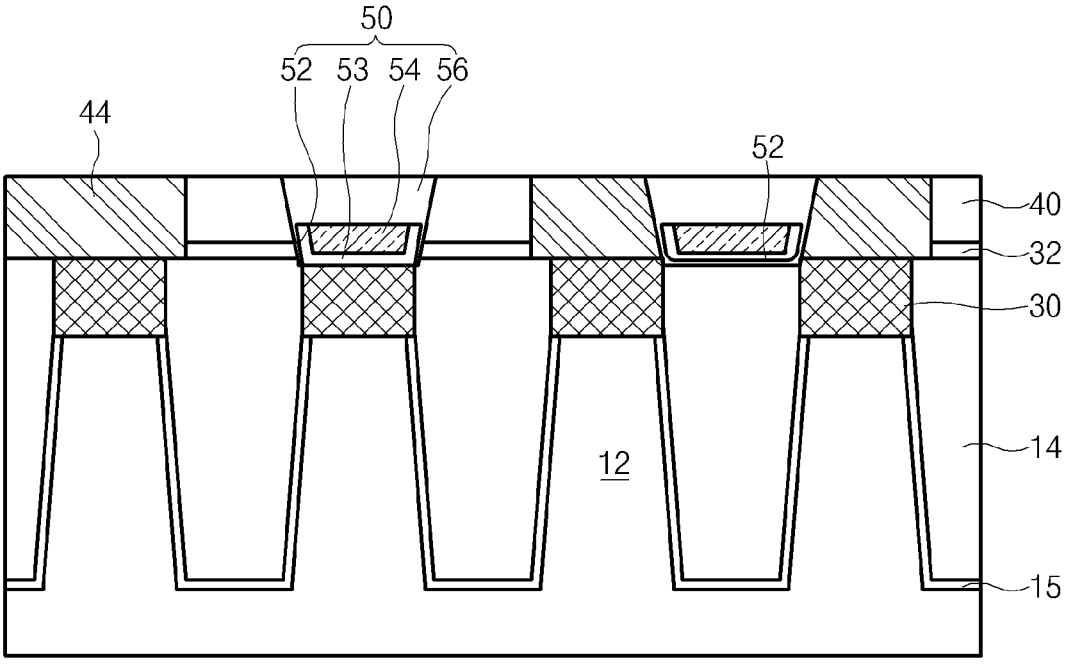
(a)


50
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(b)

Fig.13

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

The present application claims priority to Korean patent application number 10-2009-0073818, filed on 11 Aug. 2009, which is incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a method of fabricating the same; more particularly, to a semiconductor device including a buried gate, a storage node and bit lines and a method of fabricating the same.

In semiconductor memory devices, DRAM has a multiplicity of unit cells, each consisting of a capacitor and a transistor. Among them, the capacitor is used to store data temporarily, and the transistor is used to transmit data between a bit line and the capacitor in response to a control signal (word line), while using the nature of a semiconductor having variable conductivity. The transistor has a gate, a source and a drain. According to a control signal applied to the gate, the charged particles are allowed to move between the source and the drain. The movement of charged particles between the source and the drain is realized via a channel region defined by the gate.

According to a method of fabricating a conventional transistor on a semiconductor substrate, a gate is first formed over the semiconductor substrate and impurities are doped into two sides of the gate to form a source and a drain. A region between the source and drain under the gate becomes a channel region for the transistor. The transistor having such a horizontal channel region occupies a certain area of the semiconductor substrate. A high density semiconductor memory device has numerous transistors formed therein so it is difficult to reduce the size of the semiconductor memory device (or the chip size).

Decreasing the chip size allows a larger number of semiconductor memory chips to be produced per wafer, leading to an improved yield. Indeed, a number of different techniques have been used to reduce the chip size. One technique is to use a recess gate instead of a traditional planar gate having a horizontal channel region, where a recess is formed on the substrate and then forming a gate in that recess so as to obtain a channel region along the curved surface of the recess. Another technique uses a buried gate that is formed by burying the entire gate within the recess.

In such a buried gate structure, an isolation gate has been used to form a bit-line contact as well as a storage node contact in a line type. However, in doing so, the cell area may become larger than the isolation gate structure and may experience a greater leakage current than for the existing trench-type device isolation film.

Also, a buried gate structure using such a trench-type device isolation film has a disadvantage in that during the patterning of a bit-line contact, a contact hole is generally require to be patterned as a hole by dry etching. If a Critical Dimension (CD) becomes smaller in size, the contact hole pattern may not be defined on a mask. Moreover, when the contact hole needs to be etched in an active region during a subsequent etching process, the active region may not open. Increasing the CD to prevent this may cause a short problem with the storage node.

Besides, there are other problems: for example, the storage node contact has to be formed as a Self Aligned Contact (SAC) after the formation of bit lines, and a reduced contact area between the active regions and the contact increases contact resistance.

BRIEF SUMMARY OF THE INVENTION

Embodiments of the present invention are directed to providing a semiconductor device and a method of fabricating the same, wherein a storage node contact hole is made sufficiently large to facilitate the etching of a storage node contact hole with a small CD. Also, a landing plug is formed to have resistance that is lower than the plug resistance, and the SAC process is performed at the time of the bit line formation.

In one embodiment, a method of fabricating a semiconductor device, includes forming a device isolation film for defining a multiplicity of active regions in a semiconductor substrate; forming a multiplicity of buried word lines in the semiconductor substrate; forming a storage node contact hole for exposing a storage node contact region of two adjoining active regions; filling the storage node contact hole with a storage node contact plug material; forming a bit-line groove for exposing a bit-line contact region of the active region and splitting the storage node contact plug material into two; and forming a bit line into the bit-line groove. By making the storage node contact hole large, any problem caused during the etching of a storage node contact hole with a small CD can be solved, and the SAC process is no longer needed during the formation of bit lines.

The method of fabricating a semiconductor device further comprises: forming a landing plug over the bit-line contact region and storage node contact region of the active region.

The formation of the landing plug preferably comprises: before the formation of the word lines, forming a hard mask oxide and a hard mask layer over the surface of the active region; after the formation of the word lines, removing the hard mask layer and the hard mask oxide from the surface of the active region; forming a landing plug in a space of the active region from which the hard mask layer has been removed; and implanting ions into the landing plug.

The formation of the storage node contact hole preferably comprises: forming an interlayer dielectric over the semiconductor substrate including the landing plug and the word lines; and etching the interlayer dielectric with the landing plug as an etch stop layer.

The method further comprises: forming a selective epi growth (SEG) layer in the bit-line contact and storage node contact regions of the active region, so as to increase the height of a junction region (source/drain) of the active region by SEG layer to lower plug resistance and to reduce GIDL (Gate Induced Drain Leakage).

The formation of the buried word lines comprises: forming a trench in the semiconductor substrate; filling the trench with a gate conductive layer; and forming a capping layer over the gate conductive layer within the trench. In this manner, buried word lines are formed on the lower portion of the surface of the silicon substrate.

The method preferably further comprises: after the formation of the bit-line groove, forming a nitride spacer on the side walls of the bit-line groove.

Preferably, the formation of the bit lines is performed by the damascene process comprising: forming a barrier metal layer on the side walls and bottom surface of the bit-line groove; and forming a bit-line conductive layer over the surface of the barrier metal layer.

The method preferably further comprises: after the formation of the barrier metal layer, thermally oxidizing the barrier metal layer to form silicide; and removing the barrier metal layer to leave the silicide.

The surface of the landing plug has preferably the same height with the surface of the device isolation film.

The present invention method of fabricating a semiconductor device comprised of: active regions formed over a semiconductor substrate, each active region including a bit-line contact region and a storage node contact region, and a device isolation film for defining the active regions; a multiplicity of word lines buried in the semiconductor substrate; a storage node contact plug buried in a storage node contact hole that exposes the storage node contact region of the two adjoining active regions; a bit-line groove for exposing the bit-line contact region of the active region and splitting the storage node contact plug material into two; and bit lines buried in the bit-line groove, is characterized in that any problem caused during the etching of a storage node contact hole with a small CD can be solved by making the storage node contact hole large and that the SAC process is not required at the time of the formation of bit lines.

With the semiconductor device further comprising a polysilicon plug formed over the bit-line contact and storage node contact regions of the active region, plug resistance can be lowered.

With the semiconductor device further comprising a selective epi growth layer over the bit-line contact and storage node contact regions of the active region, the height of the junction region (source/drain) of the active region can be increased by the SEG layer, and this in turn lowers plug resistance and reduces GIDL.

The semiconductor device preferably further comprises an interlayer dielectric formed over the word lines and device isolation film, and the word line is formed of a buried word line comprising: a gate conductive layer buried in a trench of the semiconductor substrate; and a capping layer formed over the gate conductive layer within the trench.

The semiconductor device preferably further comprises a nitride spacer formed on the side walls of the bit-line groove, and the bit lines are formed by the damascene process comprising: forming a barrier metal layer on the side walls and bottom surface of the bit-line groove; and forming a bit-line conductive layer over the surface of the barrier metal layer.

The semiconductor device preferably further comprises silicide formed between the barrier metal layer and the bit-line conductive layer, and the surface of the landing plug has the same height as the surface of the device isolation film.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** to FIG. **13** are plan or sectional views sequentially illustrating a fabrication method of a semiconductor device according to the present invention.

DESCRIPTION OF EMBODIMENTS

Embodiments of a method of fabricating a semiconductor device according to the present invention will now be described in greater detail with reference to the accompanying drawings.

FIG. **1** to FIG. **13** are plan or sectional views sequentially illustrating a fabrication method of a semiconductor device according to the present invention. In FIG. **2**, (a) is a sectional view taken along the Y direction in FIG. **1**, (b) is a sectional view taken along the X direction in FIG. **1**. Other figures follow the same orientations.

Referring first to FIG. **1**, active regions **12** and device isolation films **14** for defining the active regions **12** are formed over a semiconductor substrate. Each active region **12** is intersected by two word lines **20**. The active region defines an acute angle with respect to the word line **20** in the present embodiment. The word line **20** is formed within the semiconductor substrate as a buried word line, i.e., the upper surface of the word line **20** is lower than the upper surface of the semiconductor substrate.

Referring to FIG. **2**, a hard mask oxide **15** and a nitride or a hard mask layer made of a polysilicon material are sequentially formed over the surface of the semiconductor substrate. The hard mask layer is etched using a mask that defines a device isolation film **14** region to form a hard mask pattern **16**. The semiconductor substrate is etched using this hard mask pattern **16** as a mask to form a trench therein, and the trench is filled with an oxide to form the device isolation film **14**.

In one embodiment, a liner nitride (not shown) and a liner oxide (not shown) are formed over the trench surface of the semiconductor substrate before the device isolation film **14** is formed thereon. The device isolation film **14** made of an oxide material is obtained by forming an oxide, e.g., using a Spin On Dielectric (SOD) method, over the entire surface of the semiconductor substrate having a trench formed therein and then removing the oxide from the surface of the hard mask pattern **16** by the CMP method to fill the device isolation film **14** into the trench.

In a conventional method, the active regions **12** were formed to have their surfaces to be the same height as the surface of the device isolation film **14**. In the present embodiment, since the hard mask **16** resides on the surface of the active regions **12**, the surface of the hard mask **16** is formed to have the same height as the surface of the device isolation film **14**, i.e., the upper surface of the active region **12** is provided to be lower than the upper surface of the device isolation **14**. This height difference between the active region **12** and the device isolation **14** facilitates the formation of a landing plug because interlayer dielectric need not be formed over the active region **12** when the hard mask pattern **16** is made of a nitride and then the nitride material is removed, or when the hard mask **16** is made of polysilicon and then the polysilicon is patterned to be used as a landing plug. In another embodiment of the present invention, instead of forming the hard mask **16** over the active region **12**, a selective epi growth (SEG) process is performed on the active region to make the surface of an SEG layer (not shown) of the active region **12** to have substantially the same height as the surface of the device isolation film **14**. In this case, although a storage node contact is formed directly on the surface of the SEG layer (not shown) over the active region **12** without forming a landing plug, since the SEG layer increases the height of a junction region (source/drain) of the active region **12**, plug resistance can be lowered and Gate Induced Drain Leakage (GIDL) is reduced.

Referring to FIG. **3**, a trench **22** having a predetermined depth for forming a buried gate **20** is formed in the semiconductor substrate having the active regions **12** and the device isolation films **14** formed thereon. The surface of the trench **22** is oxidized to form a gate oxide **24**, and the trench **22** having the gate oxide **24** formed thereon is filled with a gate electrode **26** (FIG. **4**). The gate electrode **26** includes TiN and tungsten (W) in the present embodiment. A capping film **28** for protecting the gate electrode **26** is formed over the gate electrode **26** within the trench **22**.

Referring to FIG. **5**, the hard mask layer **16** is removed and a landing plug **30** is formed in a space created by removing the hard mask layer **16**. The landing plug **30** electrically connects the junction region (source/drain) of the semiconductor sub-

strate to the bit-line contact plug and the storage node contact plug. The landing plug **20** is formed of conductive material (e.g., polysilicon). The landing plug formation process includes depositing a landing plug material such as polysilicon within the space created by the removal of the hard mask layer **16** and over the capping film **28**. Excess landing plug material that protrudes above the capping film **28** is removed using chemical mechanical polishing (CMP) or etch-back. The landing plug **30** can be formed by depositing doped polysilicon, or by depositing polysilicon and then implanting ions for doping.

Rather than forming a bit-line contact plug and a storage node contact plug directly on the junction region of the semiconductor substrate, the landing plug **30** on the junction region of the semiconductor substrate since bit lines are to be formed by the damascene process (to be described) in the present embodiment. The landing plug **30** (or an SEG layer grown on the active region **12**) couples the bit lines and the junction regions of the active region **12**. By the use of landing plug **30**, loss of the semiconductor substrate can be avoided during the damascene process used to form the bit lines. As a result, a junction region having a low depth can be utilized. In addition, since a metal plug is not formed directly on the active region, the landing plug **30** serves as a buffer, and the contact surface between the active regions **12** and the contact plug (landing plug) is increased, thereby lowering plug resistance.

A sealing nitride **32** is formed over the landing plug **30**, buried gate **20** and device isolation film **14** to protect the buried gate **20** and the landing plug **30**. A gate is formed in a peripheral region (not shown), not in the cell region that has been described thus far.

Referring to FIG. **6**, an interlayer dielectric (ILD) **40** is formed over the sealing nitride **32**.

A portion of the ILD **40** is etched to form a storage node contact hole **42** (FIG. **7**). Hole **42** exposes the landing plug **30** and is used to form a storage node contact plug. FIG. **7**(*b*) shows a cross sectional view along the X direction of the semiconductor device of FIG. **8**. The storage node contact hole **42** includes a storage node region of two adjacent active regions **12** in the present embodiment.

In a conventional method, a storage node contact hole **42** of each active region **12** is formed individually, i.e., one contact hole for each active region. In the present embodiment, one storage node contact hole **42** is formed for two adjacent active regions **12**. As a result, a bigger contact hole pattern may be used for the contact hole. The occurrence of a contact hole pattern not being defined on the mask produced during the formation of a contact hole pattern may be minimized. The storage node contact hole pattern including two storage node contact regions is split into two to electrically isolate the two, the process of which is described later.

In the present embodiment, a storage node contact plug is formed before a bit line contact plug so that the bit line formation process may proceed in a similar way with the buried gate formation process.

Referring to FIG. **9**, the storage node contact hole **42** exposing the landing plug **30** is filled with a conductive material to form a storage node contact plug **44**. This storage node contact plug **44** is made of the same material as the landing plug **30** (e.g., polysilicon) in the present embodiment. For example, after a polysilicon layer is deposited on the entire surface of the semiconductor substrate having the storage node contact hole **42** formed therein, the polysilicon layer on the upper portion of the surface of the interlayer dielectric **40** is removed by CMP or etch-back.

Referring to FIG. **10**, a hard mask pattern **55** is formed to define a bit line region over the interlayer dielectric **40** having the storage node contact plug **44** formed therein. The hard mask pattern **55** may be a nitride.

With the hard mask pattern **55** as a mask, a bit-line groove **51** for forming bit lines is etched to a predetermined depth so as to expose the surface of the landing plug **30** in a portion of the bit line region.

The bit-line groove **51** is used to form bit lines by a damascene process. The bit-line groove **51** formed also splits the storage node contact plug **44** (see FIG. **10** (*b*)) that extends across two adjacent active regions **12** into two separate pieces, where each separated piece connecting the respective active region **12**. As a result, the SAC process does not need to be used at the time of the formation of a bit-line contact hole and a storage node contact hole.

As shown in FIG. **11**, as the storage node contact plug **44** is formed in each of a multiplicity of active regions **12**, bit lines are also formed in an intersecting manner with those active regions **12**. Therefore, by forming a bit-line groove **51**, one storage node contact plug **44** formed over two active regions can be split.

Referring next to FIG. **12**, dielectric spacers **52** for insulating the bit-line groove **51** are formed on the bottom and side walls of the bit-line groove **51**. This dielectric spacer **52** is preferably made of a material having a low dielectric constant, such as a nitride or oxide.

A contact mask (not shown) opens only a bit-line contact node portion (the left side bit-line groove **51** in FIG. **12**(*b*)) where a bit-line contact is supposed to be formed so as to remove the dielectric spacer **52** on the bottom surface of the bit-line groove **51**, thereby exposing the landing plug **30**.

Referring to FIG. **13**, bit lines **50** are formed in the bit-line grooves **51** having the dielectric spacer **52** formed thereon. To be more specific, a bit-line barrier metal layer **53** is formed first on the bottom and sidewall surfaces of the bit-line groove **51**. The barrier metal layer **53** includes Ti/TiN or Ti_xSi_x material in one embodiment.

In one embodiment, the barrier metal layer **53** is thermally treated for silicidification, where an interface region is converted to silicide while the bulk material (not shown) remains non-silicided. The upper portion is removed to leave the lower portion that has been converted to silicide remaining in the bit line groove **51**. Since the portion where the bit-line contact is to be formed is free of the dielectric spacer **52**, the bit lines are electrically connected with the landing plug **30**.

A bit-line conductive layer **54** is formed over the surface of the barrier metal layer **53** (silicide in one embodiment), the bit-line conductive layer **54** may be made of tungsten (W). Meanwhile, to increase adhesion between the barrier metal layer **53** and the bit-line conductive layer **54**, an adhesive layer or TiN layer (not shown) may additionally be formed on the interface between these two layers.

A bit-line hard mask **56** made of a nitride material is formed over the barrier metal layer **53** and bit-line conductive layer **54**. The bit-line hard mask formation process includes depositing a nitride over the entire surface, and leaving the bit-line hard mask **56** only inside the bit-line groove **52** using CMP or etch-back.

Although subsequent processes are not shown, it should be understood that a capacitor consisting of a lower electrode, an upper electrode and a dielectric is formed over the storage node contact plug **44**. Additional layers are formed thereover to complete the fabrication process of a semiconductor device.

The above embodiments of the present invention are illustrative and not limitative. Various alternatives and equivalents

are possible. The invention is not limited by the embodiments described herein. Nor is the invention limited to any specific type of semiconductor device. Other additions, subtractions, or modification are obvious in view of the present disclosure and are intended to fall within the scope of the appended claims.

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

forming a device isolation structure to define a plurality of active regions in a substrate, the plurality of the active regions including first and second active regions that are provided adjacent to each other;

forming a plurality of buried word lines in the substrate, each buried word line being defined within a trench formed in the substrate;

forming a storage node contact hole extending over the first and second active regions;

filling the storage node contact hole with a storage node contact plug material;

forming a bit-line groove to split the storage node contact plug material into first and second storage node contact plugs, the first storage node contact plug being assigned to the first active region and the second storage node contact plug being assigned to the second active region; and

forming a bit line within the bit-line groove.

2. The method of claim **1**, further comprising:

forming a landing plug over the bit-line contact region and the storage node contact region.

3. The method of claim **2**, wherein the formation of the landing plug comprises:

forming a hard mask oxide and a hard mask layer over the surface of the first and second active regions before forming the buried word lines;

removing the hard mask layer and the hard mask oxide from the surface of the first and second active regions after forming the buried word lines; and

forming the landing plug in a space defined by the removal of the hard mask layer.

4. The method of claim **3**, further comprising:

implanting ions into the landing plug.

5. The method of claim **2**, wherein the formation of the storage node contact hole comprises:

forming an interlayer dielectric over the substrate including the landing plug and the word lines; and

etching the interlayer dielectric using the landing plug as an etch stop layer.

6. The method of claim **2**, wherein the surface of the landing plug has substantially the same height as the surface of the device isolation structure.

7. The method of claim **1**, further comprising:

forming a selective epi growth (SEG) layer in the bit-line contact and storage node contact regions of the first and second active regions.

8. The method of claim **1**, wherein the formation of the buried word lines comprises:

forming a plurality of trenches in the substrate;

filling the trenches with a gate conductive layer; and

forming a capping layer over the gate conductive layer within the trenches.

9. The method of claim **1**, further comprising:

forming a nitride spacer on a bottom and side surfaces of the bit-line groove; and

removing the nitride spacer from the bottom of the bit-line groove in a portion of the bit-line contact node portion.

10. The method of claim **1**, wherein the formation of the bit lines comprises:

forming a barrier metal layer on the side walls and bottom surface of the bit-line groove; and

forming a bit-line conductive layer over the surface of the barrier metal layer.

11. The method of claim **10**, further comprising:

thermally treating the barrier metal layer to convert a portion of the barrier metal layer into silicide; and

removing the barrier metal layer that was not converted to silicide, thereby leaving the silicide within the bit line groove.

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